



nanomaterials

Electronic Nanodevices

Edited by

Antonio Di Bartolomeo

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Electronic Nanodevices

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Editor

Antonio Di Bartolomeo

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Contents

About the Editor	vii
Antonio Di Bartolomeo Electronic Nanodevices Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 2125, doi:10.3390/nano12132125	1
Peng Cui and Yuping Zeng Effect of Device Scaling on Electron Mobility in Nanoscale GaN HEMTs with Polarization Charge Modulation Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 1718, doi:10.3390/nano12101718	5
Monica La Mura, Patrizia Lamberti and Vincenzo Tucci Numerical Evaluation of the Effect of Geometric Tolerances on the High-Frequency Performance of Graphene Field-Effect Transistors Reprinted from: <i>Nanomaterials</i> 2021 , <i>11</i> , 3121, doi:10.3390/nano11113121	17
Mirko Poljak, Mislav Matić, Tin Župančić and Ante Zeljko Lower Limits of Contact Resistance in Phosphorene Nanodevices with Edge Contacts Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 656, doi:10.3390/nano12040656	31
Enver Faella, Kimberly Intonti, Loredana Viscardi, Filippo Giubileo, Arun Kumar, Hoi Tung Lam, Konstantinos Anastasiou, Monica F. Craciun, Saverio Russo and Antonio Di Bartolomeo Electric Transport in Few-Layer ReSe ₂ Transistors Modulated by Air Pressure and Light Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 1886, doi:10.3390/nano12111886	43
Khalil Tamersit, Jaya Madan, Abdellah Kouzou, Rahul Pandey, Ralph Kennel and Mohamed Abdelrahem Role of Junctionless Mode in Improving the Photosensitivity of Sub-10 nm Carbon Nanotube/Nanoribbon Field-Effect Phototransistors: Quantum Simulation, Performance Assessment, and Comparison Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 1639, doi:10.3390/nano12101639	55
Khalil Tamersit, Abdellah Kouzou, Hocine Bourouba, Ralph Kennel and Mohamed Abdelrahem Synergy of Electrostatic and Chemical Doping to Improve the Performance of Junctionless Carbon Nanotube Tunneling Field-Effect Transistors: Ultrascaling, Energy-Efficiency, and High Switching Performance Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 462, doi:10.3390/nano12030462	71
Mitsue Takahashi and Shigeki Sakai Area-Scalable 10 ⁹ -Cycle-High- Endurance FeFET of Strontium Bismuth Tantalate Using a Dummy-Gate Process Reprinted from: <i>Nanomaterials</i> 2021 , <i>11</i> , 101, doi:10.3390/nano11010101	89
Juan B. Roldán, Gerardo González-Cordero, Rodrigo Picos, Enrique Miranda, Félix Palumbo, Francisco Jiménez-Molinos, Enrique Moreno, David Maldonado, Santiago B. Baldomá, Mohamad Moner Al Chawa, Carol de Benito, Stavros G. Stavrinides, Jordi Suñé and Leon O. Chua On the Thermal Models for Resistive Random Access Memory Circuit Simulation Reprinted from: <i>Nanomaterials</i> 2021 , <i>11</i> , 1261, doi:10.3390/nano11051261	103

Sara Bernardes, Ricardo A. Marques Lameirinhas, João Paulo N. Torres and Carlos A. F. Fernandes	
Characterization and Design of Photovoltaic Solar Cells That Absorb Ultraviolet, Visible and Infrared Light	
Reprinted from: <i>Nanomaterials</i> 2021 , <i>11</i> , 78, doi:10.3390/nano11010078	149
Francisco Duarte, João Paulo N. Torres, António Baptista and Ricardo A. Marques Lameirinhas	
Optical Nanoantennas for Photovoltaic Applications	
Reprinted from: <i>Nanomaterials</i> 2021 , <i>11</i> , 422, doi:10.3390/nano11020422	165
T. F. Alhamada, M. A. Azmah Hanim, D. W. Jung, A. A. Nuraini and W. Z. Wan Hasan	
A Brief Review of the Role of 2D Mxene Nanosheets toward Solar Cells Efficiency Improvement	
Reprinted from: <i>Nanomaterials</i> 2021 , <i>11</i> , 2732, doi:10.3390/nano11102732	191
Hua Wang, Tianyi Li, Ahmed M. Hashem, Ashraf E. Abdel-Ghany, Rasha S. El-Tawil, Hanaa M. Abuzeid, Amanda Coughlin, Kai Chang, Shixiong Zhang, Hazim El-Mounayri, Andres Tovar, Likun Zhu and Christian M. Julien	
Nanostructured Molybdenum-Oxide Anodes for Lithium-Ion Batteries: An Outstanding Increase in Capacity	
Reprinted from: <i>Nanomaterials</i> 2022 , <i>12</i> , 13, doi:10.3390/nano12010013	209

About the Editor

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Antonio Di Bartolomeo is a professor of Experimental Condensed Matter Physics and the president of the Physics Education Committee at the University of Salerno, Italy, where he teaches semiconductor device physics and nanoelectronics.

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Editorial

Electronic Nanodevices

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The new phenomena observed in nanodevices and the related technological challenges of fabrication and manipulation at the nanoscale have spurred intense theoretical, simulation and experimental research activity. New device structures, materials, simulation and characterization techniques have emerged.

The Special Issue entitled “Electronic Nanodevices” focuses on the design, simulation, fabrication, and modeling of new nanodevices for electronic, optoelectronic and energy applications; it includes articles dealing with nanoscale transistors, phototransistors, memories, and solar cells.

The effects of down-scaling and the introduction of new materials, architectures and fabrication processes in transistors and phototransistors are widely investigated.

High-electron-mobility transistors (HEMTs) are devices designed for high-frequency and high-power applications. An experimental study by P. Cui and Y. Zheng checked the impact of vertical and lateral scaling on low-field electron mobility in GaN HEMTs [1]. Although low-field mobility is expected to stay constant when devices scale down, in GaN HEMTs, the distribution of polarization charges that scatter with the channel electrons, localized in the barrier layer, can change with the device dimensions, thus leading to mobility variations. Indeed, P. Cui and Y. Zheng demonstrate that in InAlN/GaN HEMTs, the mobility decreases as the InAlN barrier and the gate length scale down but increases with the down-scaled source–drain distance. Their study highlights that the polarization charges are an important ingredient to consider in the nanoscale device design.

Owing to their great mechanical, electronic, and carrier transport properties, two-dimensional (2D) materials such as graphene, black phosphorus and transition metal dichalcogenides [2–6], as well as one-dimensional (1D) carbon nanotubes [7,8], are considered promising candidates for future post-silicon electronic and optoelectronic devices. Their use as channel of field effect transistors (FET) has been an important part of the down-scaling process.

M. La Mura and coworkers numerically investigated the effects of device geometry and graphene quality variations on the performance of graphene-field effect transistors (GFETs) [9]. The poor repeatability of GFETs hampers their diffusion in GFET-based commercial RF circuits. Specifically, the impact of geometrical parameters on the RF performance of a GFET-based common-source amplifier is studied in terms of the amplifier transit frequency and maximum oscillation frequency. M. La Mura and coworkers concluded that the most influential factor variation on the transition frequency and the maximum oscillation frequency is the channel length, as expected, because the transistor high-frequency limit is inversely proportional to the time the carriers need to cross the channel. They show that reducing the channel length increases the transition and the maximum frequency and point out that the accurate control the channel length is essential to reducing unwanted fluctuations of the transistors’ cut-off frequency. They also highlight that the improvement provided by increasing the accuracy of the other geometrical parameters, such as channel width or top oxide thickness, is very limited.

M. Poljak and coworkers dealt with the contact resistance in black phosphorus nanoribbons (PNRs) with edge contacts using atomistic quantum transport simulations [10]. The acceptable bandgap and the high carrier mobility of monolayer black phosphorus (or

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phosphorene) make it more advantageous than other 2D materials for nanoscale FETs. The impact of PNR size down-scaling on the contact resistance is analyzed for technologically relevant PNR widths and lengths. It is shown that the contact resistance decreases with the width down-scaling but increases considerably when the length decreases. Significant metallization effects become visible in the deterioration of electronic and transport properties for nanoribbon lengths below ~ 8 nm. It is pointed out that for optimized metal edge contacts, a weakly interacting metal is best suited to ultra-short nanoribbons. The numerical results indicate that in ultra-narrow PNR devices, the quantum intrinsic limits of the contact resistance, i.e., minimum achievable contact resistance, could be as low as $\sim 14 \Omega \mu\text{m}$, a level acceptable to the CMOS industry.

E. Faella et al. fabricated back-gated FETs based on few-layer ReSe_2 with Cr contacts and presented their optoelectronic characterization [11]. The devices show n-type conduction due to the alignment of the Cr Fermi level with the ReSe_2 conduction band. It is demonstrated that the ReSe_2 FETs are strongly affected by air pressure and undergo a dramatic increase in conductivity when the air pressure is lowered below the atmospheric pressure. The exposure to air suppresses the channel conductivity as an effect of electron capture by oxygen and water molecules adsorbed on the material surface. The reversible pressure behavior allows the devices to be used as air pressure gauges. Finally, a negative photoconductivity in the ReSe_2 channel is found and explained as back-gate-dependent trapping of the photo-excited charges.

K. Tamersit and coworkers performed numerical simulations by self-consistently solving the Poisson equation with the mode space non-equilibrium Green's function formalism in the ballistic limit to investigate carbon nanotube/nanoribbon junctionless phototransistors, endowed with sub-10 nm photogate lengths [12]. The light-induced modulation of electrostatics through the photogate is employed as a photosensing principle and the impact of the light illumination on the transport of carbon-based junctionless phototransistors is analyzed via the energy-position-resolved electron density. They find that the junctionless approach is efficient in boosting the photosensitivity of phototransistors by dilating the potential barrier while mitigating the tunneling currents and improving the subthreshold characteristics. They also compare graphene nanoribbon and carbon nanotube junctionless phototransistors, concluding that the former exhibit higher photosensitivity.

The same group in another computational work proposed an efficient approach based on the synergy of electrostatic and chemical-doping engineering to boost the subthreshold and switching performance of sub-10 nm junctionless-carbon-nanotube-tunnel field-effect transistors [13]. Their doping approach, also favored by ferroelectric-based gating, is exploited to shrink the band-to-band tunneling window and dilate the direct source-to-drain tunneling window.

Ferroelectric gates are also considered by M. Takahashi and S. Sakai who fabricated a new strontium bismuth tantalate (SBT) ferroelectric-gate FET with channel lengths of 85 nm by a replacement-gate process [14]. Their device is demonstrated to be suitable for non-volatile memories with long stable data retention of 10^5 s and high erase-and-program endurance up to 10^9 cycles. In the fabrication process, they prepared dummy-gate transistor patterns and then replaced the dummy substances with an SBT precursor which is subsequently annealed for SBT crystallization. The proposed process has good channel-area scalability in geometry depending on the lithography ability.

Memory devices are also treated in a review paper by Juan B. Roldán and coworkers, dedicated to resistive random access memories (RRAMs) [15]. RRAMs are based on resistive switching mechanisms to modulate their conductance in a non-volatile manner and exhibit a set of technological features that make them ideal candidates for applications related to non-volatile memories, hardware cryptography, and neuromorphic computing. The review is focused on RRAM models dealing with temperature effects, which are very important considering that the physical mechanisms behind resistive switching are thermally activated. The authors describe models of different complexity to integrate thermal effects in complete compact models that account for the kinetics of the chemical reactions

behind resistive switching and the current calculation. Specifically, among other issues, they treat different geometries, operation regimes, lateral heat losses, etc. to characterize each conductive filament.

Driven by the ever-increasing need for sustainable energy sources, the design, fabrication, and characterization of solar cells have also attracted a great deal of research endeavor.

S. Bernardes and coworkers numerically studied the lattice-matched GaInP/GaInAs/Ge triple-junction solar cell, which is currently being used in most satellites and concentrator photovoltaic systems [16]. They first analyzed the three subcells individually and then they simulated the whole cell by extracting the typical figures-of-merit. They compared the simulated results with the actual experimental results, confirming that the cell is emulated successfully. After that, they investigated the effect of temperature, which is relevant for space applications, and proceeded with the optimization of the cell, in terms of thickness and doping, so that the maximum efficiency can be reached. As an important guideline for fabrication, they also highlighted how the doping can significantly boost the cell efficiency.

F. Duarte and coworkers used COMSOL Multiphysics® software to study nanometric optical antennas, with dimensions smaller than the wavelength of the incident electromagnetic wave, for solar energy harvesting on photovoltaic cells [17]. The use of optical antennas has received significant interest as they represent a viable alternative to the traditional energy harvesting technologies. To increase the efficiency of solar cells, the behavior of optical aperture nanoantennas, which consist of a metal sheet with apertures of dimensions smaller than the wavelength, is studied for materials such as aluminum, gold, and platinum. With several simulations in different conditions, F. Duarte and coworkers showed that all three metals exhibit the optical transmission phenomenon, i.e., they transmit a greater amount of light than might naively be expected. The enhanced transmission is due to the coupling of light with surface plasmon polaritons on the surface of the metallic nanoantennas. Furthermore, it is shown that aluminum is superior to the other materials because of its transmission and reflection coefficients.

Efficient solar cells can also be achieved through the development of innovative materials. Among them, two-dimensional metal MXenes, consisting of transition-metal nitrides or carbides, have emerged for their outstanding transparency, metallic electrical conductivity, and mechanical characteristics. Recent applications of MXene materials in solar cells and new perspectives to achieve higher power conversion efficiency with an excellent quality–cost ratio are offered in a review paper by T. F. Alhamada and coworkers [18]. The review details the basic principles for the creation of each 2D transition-metal MXene structure, the tunable characteristics depending on the transition-metal composition and summarizes all previously reported work on incorporating MXene into solar cells. The roles that MXenes play to improve solar power generation, operational stability and power conversion efficiency are reviewed.

Efficient energy storage is another important aspect of the sustainable development. Currently, lithium-ion batteries (LIBs) have become one of the most important energy storage technologies and their progress requires the development of high-capacity electrode materials [19]. Molybdenum oxides such as MoO₂ and MoO₃ are considered as promising anode materials for LIBs due to the broad spectrum of electrical properties ranging from metallic (MoO₂) to wide band gap semiconducting (MoO₃) character. In this direction, H. Wang and coworkers used orange peel extract as an effective chelating agent to synthesize molybdenum oxides [20]. MoO₂ and MoO₃ are prepared in vacuum and in air, respectively, at a temperature of 450 °C. Extensive morphological and structural characterization along with electrical and electrochemical analysis are performed to show their outstanding properties in terms of capacity upgrading upon cycling and as an anode in material for Li-ion batteries.

In summary this Special Issue offers a good overview of the recent research in nanoscale transistors, based on 1D and 2D materials, solar cells, memory devices, and electrochemical devices.

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Article

Effect of Device Scaling on Electron Mobility in Nanoscale GaN HEMTs with Polarization Charge Modulation

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Abstract: We have experimentally investigated the impact of vertical and lateral scaling on low-field electron mobility (μ) in InAlN/GaN high-electron-mobility transistors (HEMTs). It is found that μ reduces as InAlN barrier (T_B) and gate length (L_G) scale down but increases with the scaled source–drain distance (L_{SD}). Polarization Coulomb Field (PCF) scattering is believed to account for the scaling-dependent electron mobility characteristic. The polarization charge distribution is modulated with the vertical and lateral scaling, resulting in the changes in μ limited by PCF scattering. The mobility characteristic shows that PCF scattering should be considered when devices scale down, which is significant for the device design and performance improvement for RF applications.

Keywords: GaN HEMTs; scaling; electron mobility; scattering; polarization charge

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1. Introduction

Due to the high breakdown voltage, high two-dimensional electron gas densities, and high electron saturation velocity, gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have been ideal for high-frequency and high-power applications, such as radar communications, electronic countermeasures, 5G applications, small base stations, new communication microsatellites, power transmission and automotive electronics [1–5]. Yan Tang et al. fabricated the AlN/GaN/AlGaIn double heterojunction HEMTs with fully passivation and n⁺-GaN ohmic contact regrowth technology, demonstrating a record high current/power gain cutoff frequency f_T/f_{max} of 454/444 GHz on a 20 nm-gate-length HEMT with gate–source and gate–drain spacings of 50 nm [6]. Jeong-Gil Kim et al. reported an AlGaIn/GaN HEMT structure on the high-quality undoped thick AlN buffer layer with a high breakdown voltage of 2154 V and a very high figure of merit (FOM) of $\sim 1.8 \text{ GV}^2 \cdot \Omega^{-1} \cdot \text{cm}^{-2}$ [7]. Xiaoyu Xia et al. reported a new type of AlGaIn/GaN HEMTs with a microfield plate (FP) with a breakdown voltage increase from 870 V to 1278 V by adjusting the distribution of the potential and channel electric field [8]. Maddaka Reddeppa et al. demonstrated high photoresponse and the electrical transport properties of a pristine GaN nanorod-based Schottky diode with an optimized Schottky barrier height [9]. Kedhareswara Sairam Pasupuleti et al. developed the integration of conductive polypyrrole (Ppy) and GaN nanorods for high-performance self-powered UV-A photodetectors, exhibiting superior photoresponse properties such as detectivity, responsivity, external quantum efficiency, good stability and reproducibility [10].

To further improve device performance, device scaling in GaN HEMTs is necessary [6,11,12]. The effects of scaling on short-channel effects (SECs), leakage current, electron velocity, frequency characteristics have been studied [13–18], providing insightful guidance for device design and performance improvement. However, few studies about the impact of scaling on electron mobility have been reported. In general, low-field mobility should not change when devices scale down. However, due to the spontaneous and piezoelectric polarization in GaN HEMTs, there are polarization charges in the barrier layer [19,20], which

is different from conventional transistors (Si, GaAs, et al.). The change in the polarization charge distribution is related to the device dimension and can result in scattering on the channel electrons [21,22], which leads to a possible change in mobility with device scaling. In this article, to demonstrate this influence, the InAlN/GaN HEMTs with various barrier thicknesses, source–drain distances, and gate lengths are fabricated and the effect of scaling on electron mobility is studied.

2. Experiment

The lattice-matched $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ HEMT structure is grown by metal–organic chemical vapor deposition on a Si substrate, as shown in Figure 1, consisting of a 2 nm GaN cap, an InAlN barrier, a 1 nm AlN interlayer, a 15 nm GaN channel layer, a 4 nm $\text{In}_{0.12}\text{Ga}_{0.88}\text{N}$ back-barrier and a 2 μm undoped GaN buffer. Here, two different InAlN layers with the thicknesses of 8 nm and 5 nm are grown. The device process started with mesa isolation with Cl_2 -based inductively coupled plasma (ICP) etching. Then, Ohmic contact was formed with Ti/Al/Ni/Au metal deposition and annealed at 850 °C for 40 s. Ni/Au gate Schottky contact was deposited in the center of the source–drain region to complete the process. For the large devices, the gate length (L_G), gate–source distance (L_{GS}), and gate–drain distance (L_{GD}) of the devices are all 2 μm . For the RF devices, two types of devices are fabricated. For type I, L_G of the devices is fixed at 50 nm and L_{SD} is 2, 1, and 0.6 μm , respectively. For type II, L_{SD} of the devices is fixed at 1 μm and L_G is 50, 100, and 150 nm, respectively. Here, the gate of all the devices is located between the source and drain regions, and the gate width is $2 \times 20 \mu\text{m}$. The current–voltage (I – V) and capacitance–voltage (C – V) measurements were carried out by using an Agilent B1500A semiconductor parameter analyzer (Agilent Technologies, Santa Clara, CA, USA).

Source	Gate	Drain
GaN (2 nm)		
InAlN (5 nm or 8 nm)		
AlN (1 nm)		
GaN (20 nm)		
InGaN (4 nm)		
GaN buffer (2 μm)		
Si Substrate		

Figure 1. Schematic cross-section of the fabricated InAlN/GaN HEMT with two different InAlN barrier thickness (8 nm and 5 nm, respectively).

3. Results and Discussion

Figure 2a,b show the measured capacitances (C) of the InAlN/GaN circle diodes with both InAlN barrier thicknesses (T_B). Here, six devices are measured and a good consistency is presented. An improved C and a subthreshold voltage (V_T) shift are observed due to the reduced InAlN barrier thickness ($C = \epsilon/T_B$, ϵ is the dielectric constant of InAlN barrier). Through integrating C – V curves, electron density (n_{2D}) is extracted as shown in Figure 2c,d. It shows that the InAlN/GaN heterostructure with 8 nm InAlN barrier presents higher electron density. Figure 3 shows the simulated band structure and 2DEG electron density as a function of the distance from the material surface of the InAlN/GaN heterostructure, which is calculated by self-consistently solving Schrodinger’s and Poisson’s equations [23,24]. Compared with the 5 nm InAlN barrier, the InAlN/GaN heterostructure with an 8 nm InAlN barrier also shows a higher electron density peak. In GaN HEMTs, the surface states are identified as the source of channel electrons. Due to the spontaneous

polarization field, the increase in InAlN barrier thickness can increase the energy of the surface states, resulting in higher electron density [25,26].

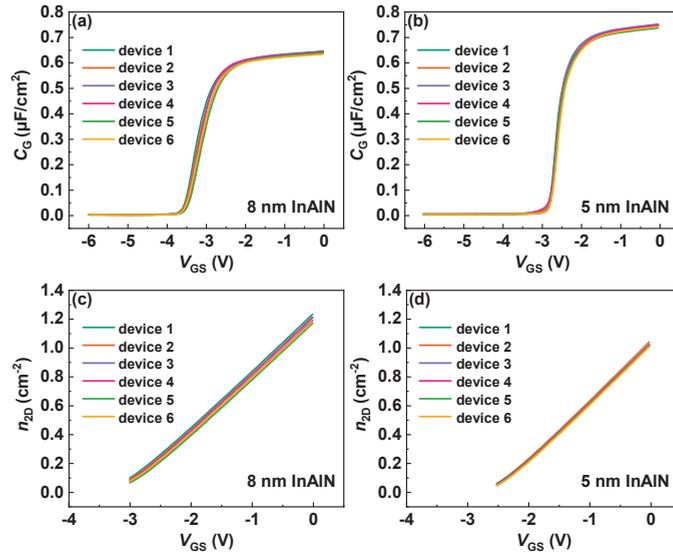


Figure 2. Gate capacitance (C_G) of the InAlN/GaN diode with (a) 8 nm InAlN and (b) 5 nm InAlN, respectively. Two-dimensional electron gas electron density (n_{2D}) of the InAlN/GaN diode with (c) 8 nm InAlN and (d) 5 nm InAlN, respectively.

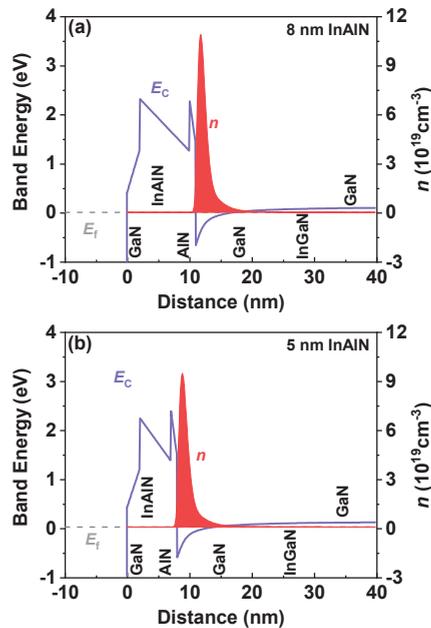


Figure 3. Simulated band structure and 2DEG electron density as a function of the distance from the material surface of the InAlN/GaN heterostructure with (a) 8 nm InAlN and (b) 5 nm InAlN, respectively.

Figure 4 shows the output characteristics of the InAlN/GaN HEMTs with different InAlN thickness. The L_G , L_{GS} , and L_{GD} of the devices are all 2 μm . To extract low-field mobility, the drain current (I_D) at $V_{DS} = 0.1$ V in the output characteristics are used. At $V_{GS} = 0$ V, the total source–drain resistance (R_{SD}) can be written as

$$R_{SD} = \frac{V_{DS}}{I_{DS}} = 2R_C + \frac{L_G + L_{GS} + L_{GD}}{n_{2D0}q\mu_0} \quad (1)$$

where R_C is the ohmic contact resistance, q is the electron charge, and μ_0 and n_{2D0} are the electron mobility and electron density under the gate region with $V_{GS} = 0$ V. Here, only μ_0 and R_C are unknown. Electron mobility in GaN HEMTs is limited by polar optical phonon (μ_{POP}), polarization Coulomb field (μ_{PCF}), acoustic phonon (μ_{AP}), interface roughness (μ_{IFR}), and dislocation (μ_{DIS}) scatterings [22,27,28]. PCF scattering is related to the nonuniformity of polarization charge distribution [21,22]. At $V_{GS} = 0$ V, the polarization charge distribution is uniform, and the PCF can be neglected. Based on the two-dimensional (2D) scattering theory and the obtained n_{2D0} [27], μ_0 can be calculated with $1/\mu_0 = 1/\mu_{POP} + 1/\mu_{AP} + 1/\mu_{IFR} + 1/\mu_{DIS}$, and then R_C can be determined with (1). Based on the obtained n_{2D0} and μ_0 , the electron mobility μ under the gate region under different V_{GS} can be extracted from

$$\frac{V_{DS}}{I_{DS}} = 2R_C + \frac{L_G}{n_{2D}q\mu} + \frac{L_{GS} + L_{GD}}{n_{2D0}q\mu_0} \quad (2)$$

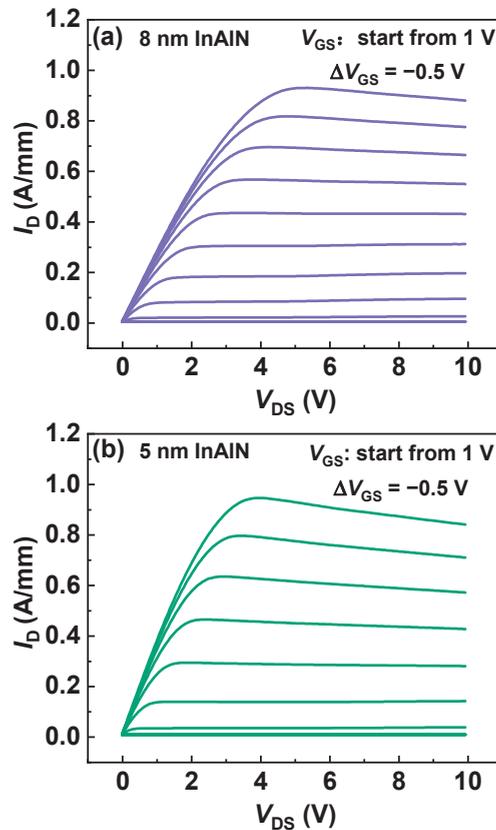


Figure 4. Output characteristics of the InAlN/GaN HEMTs with (a) 8 nm InAlN and (b) 5 nm InAlN, respectively.

Figure 5 depicts the extracted μ versus V_{GS} for both samples. At $V_{GS} = 0$ V, μ of the devices with 8 nm InAlN and 5 nm InAlN is 1221 and 1651 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. The improved electron mobility with a thinner barrier is also confirmed with the Hall measurement (1242 $\text{cm}^2/\text{V}\cdot\text{s}$ for 8 nm InAlN and 1663 $\text{cm}^2/\text{V}\cdot\text{s}$ for 5 nm InAlN) and the electron mobility of Fat-FETs (with L_G of 96 μm and L_{SD} of 100 μm , 1101 $\text{cm}^2/\text{V}\cdot\text{s}$ for 8 nm InAlN and 1670 $\text{cm}^2/\text{V}\cdot\text{s}$ for 5 nm InAlN) [29].

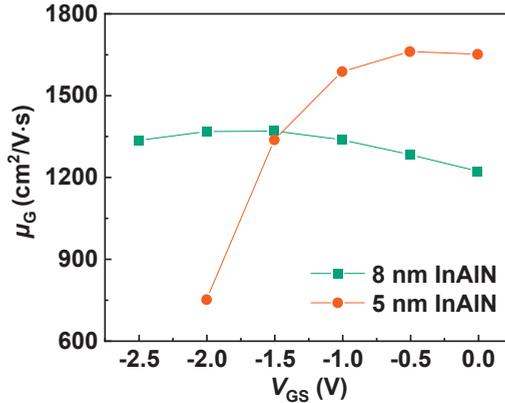


Figure 5. Extracted μ versus V_{GS} of the devices with 8 nm and 5 nm InAlN.

As shown in Figure 5, μ presents a different trend versus V_{GS} for the devices with different InAlN thickness. As V_{GS} increases, μ of the device with 8 nm InAlN decreases, but that of the device with 5 nm InAlN increases. Figure 6a,b show the calculated μ limited by different scatterings for both devices [21,30,31]. The calculated μ (μ_{CAL} , lines in the figures) by using 2D scattering theory shows good agreement with the extracted μ (scatters in the figures), which proves the accuracy of the calculation. As V_{GS} increases, μ_{POP} and μ_{IFR} decrease, μ_{DIS} and μ_{PCF} increase, and μ_{AP} presents a slight change. μ_{POP} and μ_{PCF} play more significant roles among all the scatterings. Figure 7 compares μ_{POP} and μ_{PCF} for both devices. When the InAlN barrier decreases from 8 nm to 5 nm, μ_{POP} increases while μ_{PCF} decreases. The reduced n_{2D} with a 5 nm InAlN barrier decreases the collision probability between channel electrons and polar optical phonons (POPs), resulting in the improved μ_{POP} [27,28]. Due to the spontaneous polarization, there are polarization charges (ρ_0) in the InAlN barrier near the InAlN/GaN interface. When V_{GS} is applied on the gate terminal, the polarization charges (ρ_G) under the gate region are changed due to the inverse piezoelectric effect [32], as shown in Figure 8. The polarization charge distribution is not uniform, and the potential periodicity is broken, resulting in polarization Coulomb field (PCF) scattering. The PCF scattering potential is from the additional polarization charges ($\sigma = \rho_0 - \rho_G$) and is written as [21,22]

$$V(x, y, z) = -\frac{q}{4\pi\epsilon} \int_{-L_{GS}-\frac{L_G}{2}}^{\frac{L_G}{2}} dx' \int_0^{W_G} \frac{\sigma}{\sqrt{(x-x')^2+(y-y')^2+z^2}} dy' - \frac{q}{4\pi\epsilon} \int_{\frac{L_G}{2}}^{\frac{L_{GD}}{2}+\frac{L_G}{2}} dx' \int_0^{W_G} \frac{\sigma}{\sqrt{(x-x')^2+(y-y')^2+z^2}} dy' \quad (3)$$

where ϵ is the dielectric constant of GaN and W_G is the gate width. Based on inverse piezoelectric effect, σ can be calculated by using $\sigma = \rho_0 - \rho_G = -ne_{33}^2 V_{GS}/(C_{33}d)$ [32]. n is the fitting parameter, and e_{33} and C_{33} are the piezoelectric coefficient and the elastic stiffness tensor of InAlN, respectively. d is the gate-to-channel distance, which is the sum of the thicknesses of the GaN cap layer (2 nm), InAlN barrier (8 or 5 nm), and AlN interlayer (1 nm). Figure 9 depicts the calculated σ versus V_{GS} with an 8 and 5 nm InAlN barrier. σ increases with the decreased T_B and V_{GS} , resulting in the enhanced PCF scattering as the

InAlN barrier thickness and V_{GS} decrease. Therefore, μ_{PCF} increases with V_{GS} . Because the device with a 5 nm InAlN barrier shows an enhanced PCF scattering, μ increases with V_{GS} . This fact is more pronounced, especially in the more negative V_{GS} region. For the device with an 8 nm InAlN barrier, the PCF scattering became weaker and the POP scattering dominates μ , leading to a slight decrease in μ when V_{GS} increases.

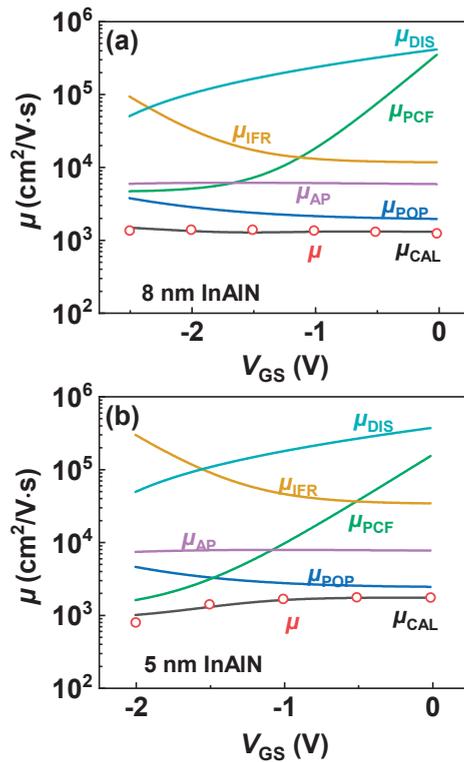


Figure 6. (a,b) Calculated μ limited by different scattering mechanisms, extracted μ (μ , scatters), and calculated μ (μ_{CAL} , lines) versus V_{GS} of both samples.

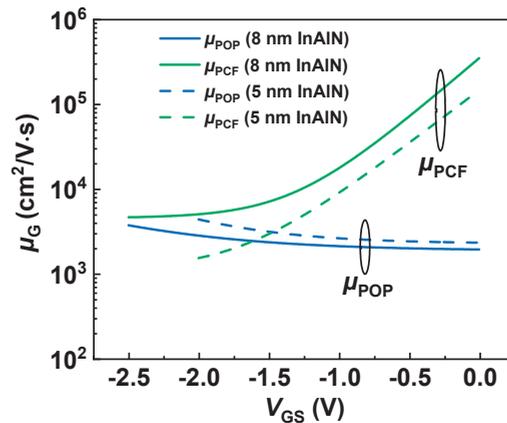


Figure 7. Comparison of μ_{POP} and μ_{PCF} versus V_{GS} of both samples.

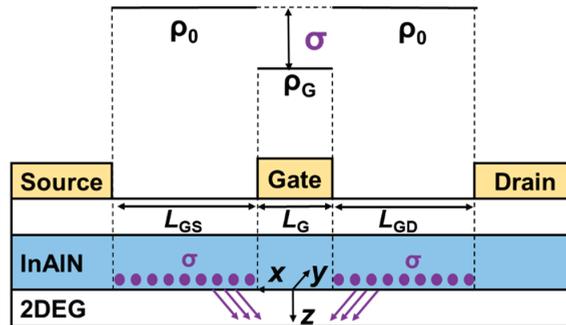


Figure 8. Schematic of the additional polarization charge (σ) distribution in InAlN barrier.

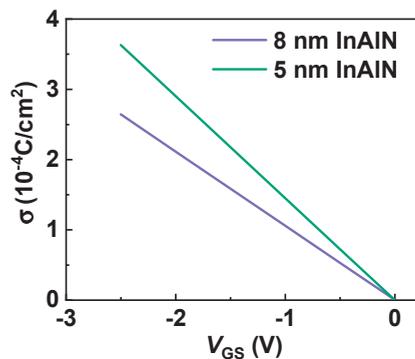


Figure 9. Additional polarization charge (σ) versus V_{GS} with 8 nm and 5 nm InAlN barrier.

From the above discussions, the vertical scale will increase σ and thus enhance PCF scattering, leading to a reduced μ . The lateral scaling is also experimentally investigated on the devices by varying L_{SD} and L_G using the same electron mobility extraction methodology. As the device laterally scales, n_{2D} is not changed, so POP, AP, IFR, and DIS scatterings are not affected. Only PCF scattering can be changed due to the modulation of the polarization charge distribution. Figure 10a,b present μ versus V_{GS} at $V_{DS} = 0.1$ V for the devices with L_G of 50 nm and L_{SD} of 2, 1, 0.6 μm with 8 nm and 5 nm InAlN. μ presents an increase with the decrease in L_{SD} . The corresponding μ_{PCF} is also calculated and plotted in Figure 10c,d. As shown in Figure 11a,b, as L_{SD} scales down, the number of σ is reduced and the effect of σ on the electron under the gate region is weakened, resulting in the increased μ_{PCF} and μ . Because PCF scattering in the device with 8 nm InAlN is weaker, the increase in μ due to the downscaling of L_{SD} is more significant. Here, μ of the devices with L_G of 2 μm is also plotted for comparison, and a significant decrease in μ in the device with an L_G of 50 nm is observed. Although the number of σ is the same under the same V_{GS} , the effect of σ on the 50 nm gate is stronger and thus PCF scattering is enhanced, leading to a decreased μ .

Figure 12a,b present the μ versus V_{GS} for the devices with L_{SD} of 1 μm and L_G of 50, 100, 150 nm with 8 nm and 5 nm InAlN. The electron mobility of all devices presents an increase with V_{GS} . This means PCF scattering plays a dominant role in the electron mobility. As V_{GS} increases from a negative value to 0 V, the electric field under the gate region decreases, resulting in the increase in μ_{PCF} and μ . For the devices with different gate lengths, μ presents an increase as L_G increases. This means the increase in gate length can increase the electron mobility. To explain this phenomenon, the corresponding μ_{PCF} is calculated and plotted in Figure 12c,d. It shows that the increase in L_G can weaken PCF scattering and increase μ_{PCF} . Because L_{SD} is fixed, as shown in Figure 13, the decreased L_G means the increased L_{GS} and L_{GD} , resulting in the enhanced effect of σ on the electrons

under the gate region. Thus, PCF scattering becomes stronger and μ reduces with the downscaled L_G .

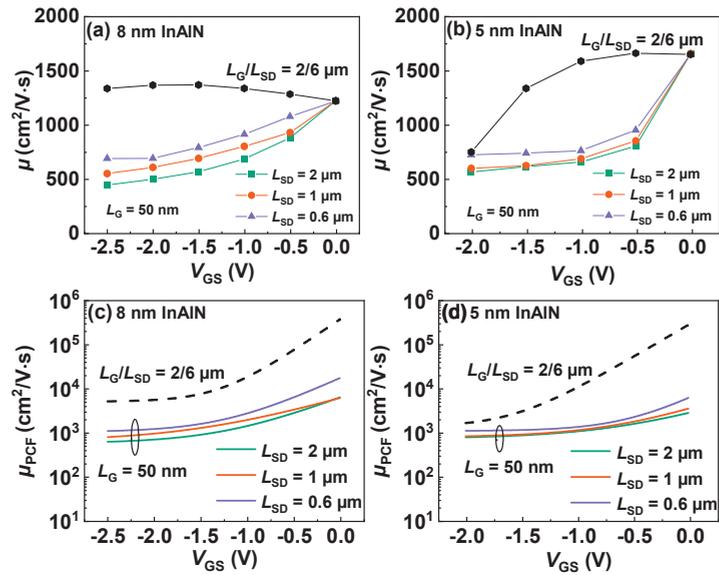


Figure 10. μ versus V_{GS} for the devices with L_G of 50 nm and L_{SD} of 2, 1, 0.6 μm with (a) 8 nm and (b) 5 nm InAlN. The device with L_G/L_{SD} of 2/6 μm is also plotted for comparison. Calculated μ_{PCF} versus V_{GS} for the same devices with (c) 8 nm and (d) 5 nm InAlN. The device with L_G/L_{SD} of 2/6 μm is also plotted for comparison.

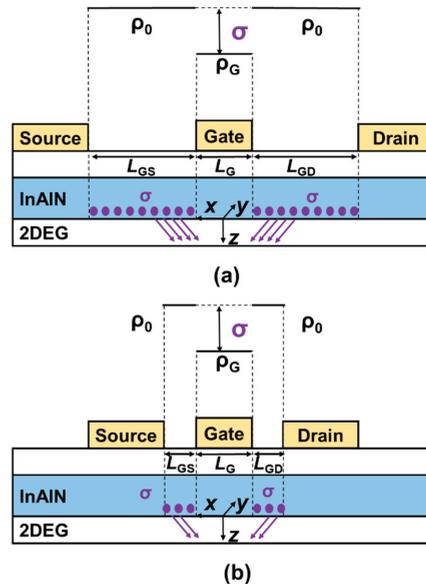


Figure 11. Schematic of the additional polarization charge (σ) distribution in InAlN barrier with (a) large and (b) small source–drain spacing L_{SD} . The gate length is fixed.

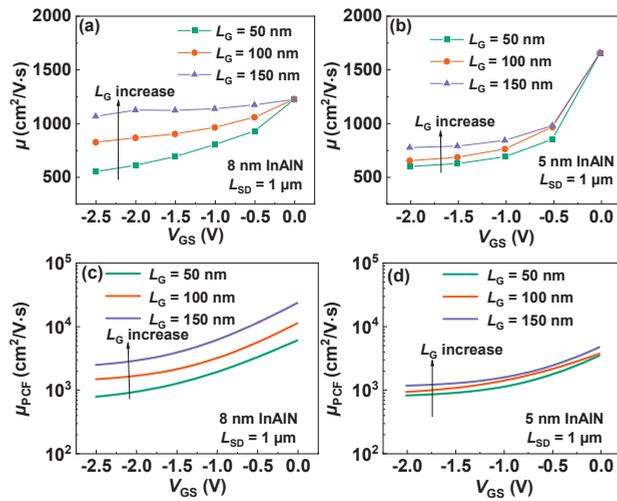


Figure 12. (a,b) μ versus V_{GS} for the devices with L_{SD} of 1 μm and L_G of 50, 100, 150 nm with 8 nm and 5 nm InAlN. (c,d) Calculated μ_{PCF} versus V_{GS} of the same devices with 8 nm and 5 nm InAlN.

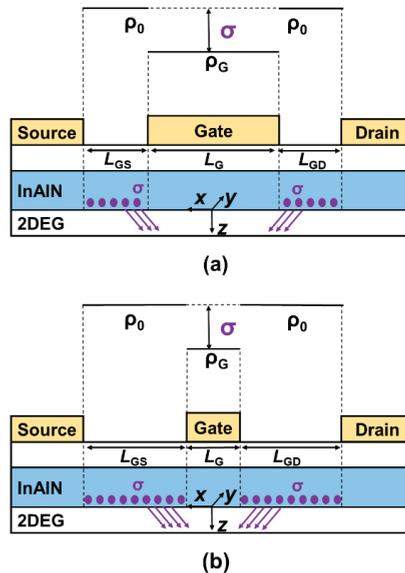


Figure 13. Schematic of the additional polarization charge (σ) distribution in InAlN barrier with (a) large and (b) small gate length L_G . The source–drain spacing L_{SD} is fixed.

4. Conclusions

In summary, the effect of down-scaling on electron mobility is experimentally demonstrated. It shows that the downscaling of barrier thickness and L_G results in a decrease in μ , but downscaled L_{SD} leads to an increase in μ . This is because the polarization charge distribution is modulated with the vertical and lateral scale, resulting in a change in PCF scattering. When GaN HEMTs scale down, the effect of PCF scattering should be considered, providing an insightful guidance for the device geometry design and performance improvement for RF application.

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Article

Numerical Evaluation of the Effect of Geometric Tolerances on the High-Frequency Performance of Graphene Field-Effect Transistors

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Abstract: The interest in graphene-based electronics is due to graphene's great carrier mobility, atomic thickness, resistance to radiation, and tolerance to extreme temperatures. These characteristics enable the development of extremely miniaturized high-performing electronic devices for next-generation radiofrequency (RF) communication systems. The main building block of graphene-based electronics is the graphene-field effect transistor (GFET). An important issue hindering the diffusion of GFET-based circuits on a commercial level is the repeatability of the fabrication process, which affects the uncertainty of both the device geometry and the graphene quality. Concerning the GFET geometrical parameters, it is well known that the channel length is the main factor that determines the high-frequency limitations of a field-effect transistor, and is therefore the parameter that should be better controlled during the fabrication. Nevertheless, other parameters are affected by a fabrication-related tolerance; to understand to which extent an increase of the accuracy of the GFET layout patterning process steps can improve the performance uniformity, their impact on the GFET performance variability should be considered and compared to that of the channel length. In this work, we assess the impact of the fabrication-related tolerances of GFET-base amplifier geometrical parameters on the RF performance, in terms of the amplifier transit frequency and maximum oscillation frequency, by using a design-of-experiments approach.

Keywords: design of experiments; GFET; graphene; high-frequency; RF devices; tolerance analysis

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1. Introduction

The research in high-frequency electronics has been historically driven by the development of advanced radiofrequency (RF) wireless telecommunication systems.

Despite the advances in CMOS-based RF devices, unsolved issues related to losses and noise have determined the rise of III-V compound semiconductors technology, which made great achievements in high-frequency applications thanks to high electron mobility [1–4]. Meanwhile, graphene has already proven to have remarkable electron mobility and thermal conductivity, and the issues related to its zero-bandgap (that prevents graphene-based devices from turning off completely) are of secondary importance in analogue RF electronics [5–9]. Hence, a great number of graphene field effect transistors (GFETs) [6,10] has been proposed, pursuing a clear current saturation [11–13] and improved voltage gain [8,14] targeting RF applications [15–21], and demonstrating the capabilities of graphene-based RF electronics. As of now, cut-off frequencies in the range of $f_T = 100\text{--}300$ GHz [16,22], and above [23] have been experimentally demonstrated for GFETs, in line with the best silicon-based FETs. The GFET maximum oscillation frequency, though, is strongly limited below 70 GHz [20,24] by the poor current saturation, the high graphene/metal contact resistance at the Gate terminal [25–27], and the unclean graphene transfer process. Exceptionally, values as high as $f_{MAX} = 200$ GHz [28] were measured, which continue to be lower than the values theoretically achievable with graphene-based devices.

Even though these results are not comparable to the best-performing III-V HEMTs, graphene RF devices are still considered appealing due to the possibility of taking advan-

tage of the GFET current ambipolarity, which enables a strong reduction in the transistor count and favours additional miniaturization capabilities [29]. This feature is extremely interesting, for example, for the aerospace field, particularly because it is accompanied by graphene's inherent tolerance to radiation [30–32]. For these reasons, several examples of graphene-based RF devices have been proposed in recent years, including antennas [33,34], transmitters and receivers [35–37], modulators and demodulators [38–43], shields [44], power and signal amplifiers [45–48], mixers [49–51], and oscillators [52–54]. Important milestones were recently reached towards the large-scale fabrication of graphene electronic devices [55] and their integration into traditional semiconductor fabrication lines [56]. On this basis, graphene can be considered very promising for the development of breakthrough RF electronics.

In this scenario, one important challenge to address is the reliability of fabricated devices. The uncontrollable variations related to the manufacturing process tolerances determine an unavoidable non-uniformity across the devices, both fabricated on different wafers and on the same wafer. This inter-wafer and intra-wafer variability of the characteristics of the fabricated devices affects the uniformity of the performance of the fabricated devices. The process-related variations of nanomaterial-based electronic devices can be gathered in two categories of factors: factors related to the layout definition, and factors related to the material properties, as stated in [57]. The first category includes the geometrical parameters defined by the lithography (for the lateral dimensions) or by the growth/deposition process (for the vertical dimensions). The second category includes the parameters expressing the graphene quality (i.e., mobility, doping caused by traps and impurities, defects), which are determined by the capability of the growth or transfer process to not degrade the material electrical properties. These two categories of factors are independent and can be treated separately. In this paper, we focus on the first category of parameters.

Extracting a mathematical relationship between the GFET parameters variability and the performance variability, e.g., in the form of a regression model, is useful to predict the uncertainty resulting from the wafer processing. To optimize the number of runs necessary to get accurate modelling of the performance variation, design of experiments (DoE) techniques can be used [58–60].

In this work, we perform a tolerance analysis of a GFET common-source amplifier, originally proposed in [45] as the first high-frequency voltage amplifier obtained by using large-area CVD-grown graphene. The device performance is assessed by means of circuit simulations, designed according to a full factorial design of experiments, and performed using a large-signal charge-based compact model of a GFET described and validated in [61]. The Advanced Design System® (Keysight Technologies, Inc., Santa Rosa, CA, USA) simulation environment is used by varying channel width, W , the channel length, L , and the top oxide thickness, t_{OX} , in order to investigate the impact of geometry variations caused by the fabrication of process-related tolerances. Following the study presented in [62], where we discussed the impact of tolerances on the amplifier's transconductance, g_m , and output conductance, g_{ds} , the influence of the same variations is reported here on the high-frequency performance described in terms of f_T and f_{MAX} .

2. GFET Simulation Design

2.1. Input Parameter Space

The geometrical parameters determine the device input capacitance, output capacitance, and trans-capacitance, which limit the high-frequency performance of a field-effect transistor. In particular, the capacitances depend on the channel width, W , the channel length, L , and the top gate oxide thickness, t_{OX} . The unevenness of these parameters, thus, impairs the uniformity of the fabricated devices' high-frequency capabilities. In [57], it was observed that FETs based on nanowires and nanotubes are more robust to process-related geometry variations as compared to bulk silicon-based MOS devices and FinFETs, from the point of view of the direct current and of the input capacitance; the impact of

the same parameters on the drain-source current of a GFET was assessed in [63]. Concerning graphene-based devices, the range of variation that should be considered for the geometrical factors is very process-dependent. The channel area is affected by an uncertainty generated either by the graphene sheet irregular shape (in the case of mechanical exfoliation and transfer of graphene flakes) [64], or by the lithography and/or etching steps (in the case of large-area CVD-grown graphene transfer) [65]. The accuracy of the thickness of the top-gate oxide depends on the thickness control capabilities of the growth or deposition technique and on the resulting roughness, and is also affected by inherent process variations [66].

In this work, the factors chosen for the tolerance analysis are W , L , and t_{OX} , and in the absence of an initial estimate of the process tolerances, a variation $\pm\Delta$ within the 10% of the nominal value is considered for each factor, in analogy with the approach proposed in [62,63,67–69].

The response variables of interest were computed in correspondence of all the combinations of the minimum value, centre value, and maximum value of each input factor, following a 3-factors, 3-levels full-factorial design of simulations. Hence, $3^3 = 27$ combinations of the input settings were considered. This approach allows accounting for simultaneous variations of all the considered input factors, enabling the investigation of possible interaction effects between the factors. In the proposed analysis, the factors are represented in the form of coded variables $x_{i,c}$, where the minimum, nominal, and maximum values are represented by the values -1 , 0 , and 1 , to provide an immediate matching with the regression model coefficients [60]. Including the centre point allows assessing the linearity of the response variable, with the scope of selecting the most suitable order for the regression model.

Table 1 reports the minimum, nominal, and maximum values of the simulation input parameters. The centre values for the three factors W , L , t_{OX} refer to the nominal design of the device described in [45] and investigated in [62,70].

Table 1. Input factors levels in the performed simulations.

	Factor	Minimum	Nominal [45]	Maximum
x_1	W (μm)	27	30	33
x_2	t_{OX} (nm)	3.6	4	4.4
x_3	L (μm)	0.45	0.5	0.55
	Coded	-1	0	-1

2.2. Output Regression Model

The chosen performance indicators, computed in correspondence of the n_c combinations of the input factors, are processed in accordance with the design of experiments techniques to evaluate the regression model coefficients. Depending on the linearity of the response variation with respect to the $m = 3$ factors $x_{i,c}$, the regression model for the performance y obtainable from the 3-by-3 full factorial plan of simulation can be [60]:

- A first-order model, including only the linear dependence on the factors (main effects model):

$$y \approx y_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_3 x_3 \quad (1)$$

- A first-order model with interactions, including a small curvature in the response by means of the mixed product terms:

$$y \approx y_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_3 x_3 + \beta_{12} x_1 x_2 + \beta_{23} x_2 x_3 + \beta_{31} x_3 x_1 \quad (2)$$

- A second order model, including quadratic terms (response surface model):

$$y \approx y_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_3 x_3 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + \beta_{33} x_3^2 + \beta_{12} x_1 x_2 + \beta_{23} x_2 x_3 + \beta_{31} x_3 x_1 \quad (3)$$

2.3. Response Variables

To assess the high-frequency operation capabilities of RF devices, the most common figures of merit are the transition frequency, f_T , and the maximum oscillation frequency, f_{MAX} .

In particular, f_T is defined as the frequency at which the current gain with the output in the short circuit condition reaches unity. By representing the common-source amplifier with a two-port network in which the input port is the gate-source terminal pair and the output port is the drain-source pair, the short-circuit current gain is the h_{21} parameter, which can be computed from the scattering parameters (*S*-parameters) matrix according to [71]:

$$h_{21} = -2S_{21} [(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}]^{-1} \quad (4)$$

The computation of the *S*-parameters is preferred because their evaluation does not require short-circuiting or open circuiting the input and output ports. These conditions are never satisfied perfectly at very high frequencies.

Despite its common use, f_T is not the most important figure of merit [72] in RF electronics. Amplifiers are useful as long as they are able to deliver power to the load, rather than current, and for this reason, it is important to also evaluate the transistor's f_{MAX} . This parameter is the frequency at which the maximum available gain (MAG), the frequency-dependent maximum power that can be transferred to the load in the impedance matching condition, reaches unity. f_{MAX} is, thus, the frequency over which the transistor is not able to amplify the input power in any case. This frequency is also called the maximum oscillation frequency because it is the frequency at which the transistor can trigger and sustain stable oscillations in oscillator circuit design. f_{MAX} is usually lower than f_T , and the most interesting frequency between the two depends on the application.

2.4. Simulation Environment Setup

To assess the impact of the fabrication-related tolerance affecting the geometrical parameters on a GFET-based amplifier RF performance, a GFET small-signal model [73,74] can be used to compute the quantities of interest according to [6,29,73]

$$f_T = \frac{g_m}{2\pi \left\{ (C_{gs} + C_{gd}) [1 + g_{ds}(R_S + R_D)] + C_{gd}g_m(R_S + R_D) \right\}} \quad (5)$$

$$f_{MAX} = \frac{g_m}{4\pi (C_{gs} + C_{gd}) \left[g_{ds}(r_i + R_S + R_G) + g_m R_G \frac{C_{gd}}{C_{gs} + C_{gd}} \right]^{1/2}} \quad (6)$$

where C_{gs} is the gate-source capacitances and C_{gd} is the drain-source capacitance, R_S , R_D , R_G , are the source, drain, and gate resistances, and $r_i = 1/(2g_m)$ is the intrinsic resistance [75].

Nevertheless, compact models for the simulation of the GFET electrical behaviour in large-signal operations have been developed and made compatible with most circuit simulators [61,76–78]. In this work, we use the charge-based large-signal GFET compact model presented in [61] and written in the hardware description language Verilog-A. This model preserves charge conservation and considers non-reciprocal self-capacitances and transcapacitances, contrarily to the Meyer's and Meyer-like models commonly used [61]. The simulated device is the GFET common-source amplifier, made of high-quality single-layer CVD-grown graphene transferred onto a silicon oxide substrate, with an ultrathin high-*k* dielectric gate oxide [79] and a 6-finger embedded gate, presented in [45] as the first high-frequency voltage amplifier obtained by using large-area graphene and already simulated in [62,70]. The compact model used for the circuit simulations requires setting the input parameters related to the geometry, to the oxide material properties, and to the graphene characteristics. The nominal settings were obtained by Pasadas et al. in [70] by fitting the experimental I–V curve reported in [45], and are listed here in Table 2.

Table 2. Input parameters of the circuit model at the nominal design point.

Parameter	Value [70]	Description
L	0.5 μm	Channel length
W	30 μm	Channel width
t_{ox}	4 nm	Top oxide thickness
ϵ_{top}	12	Top oxide relative permittivity
V_{GS0}	0.613 V	Top gate voltage offset
Δ	0.095 eV	Electrostatic potential inhomogeneity due to electron-hole puddles
$\hbar\omega$	0.12 eV	Effective energy of substrate optical phonon emission
μ	4500 cm^2/Vs	Effective carrier mobility

Concerning the resistance at the transistor’s terminals, they are taken into account by adding external lumped resistors. In [70], the values indicated for the drain and source contact resistances R_D and R_S for the nominal design of the considered device are dependent on the channel width and equal to $R_D = R_S = 435 \Omega \mu\text{m}$, whereas the gate resistance R_G is a fixed resistance $R_G = 14 \Omega$. Nevertheless, the contact resistance is known to impact strongly on the high-frequency limits of the GFET [80]. Therefore, in the performed simulations, the drain and source resistances and the gate resistance are increased proportionally to the channel width and to the channel length, respectively, in order to include the effect of the geometry variation. On the contrary, the dependence of the contact resistance upon other parameters related to the channel transport properties at different field intensities are not addressed here, since these properties are not related to the geometrical parameters that are the focus of this paper.

The circuit schematic can be seen in Figure 1.

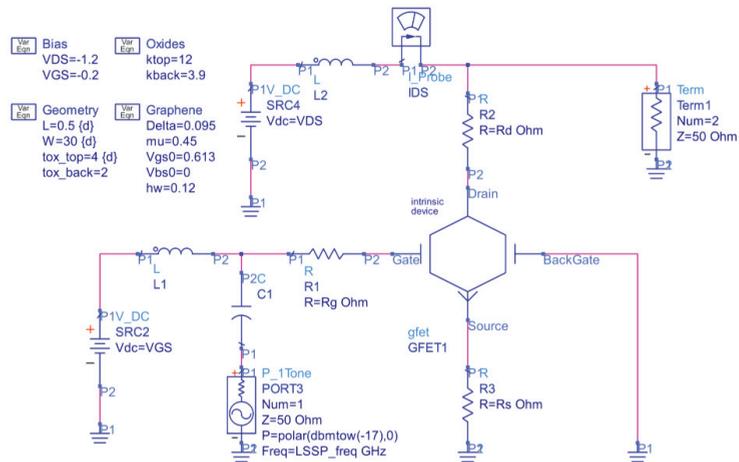


Figure 1. Schematic for the GFET amplifier large-signal S -parameters (LSSP) analysis.

Simulations are run in the Advanced Design System—ADS (®Keysight, Inc., Santa Rosa, CA, USA) software environment, which performs a DC analysis to choose the bias point and large-signal S -parameters (LSSP) analysis to take into account the device nonlinearity in the computation of the S -parameters. Figure 2 shows the drain current I_D computed by varying the drain-source and gate-source bias voltage. As can be observed by viewing the surface curvature, the saturation of the drain current can be obtained in a certain bias region. Since the choice of the bias point is of great importance to achieve optimum performance [81], it was carefully chosen to achieve the maximum intrinsic voltage gain $A_V = g_m g_{ds}^{-1}$. Searching for the optimal bias point, the applied V_{DS} was intentionally limited to prevent the effects of the carrier velocity saturation and the possible

self-heating that intervene in high-field conditions, as these phenomena are not addressed by the model. On this basis, the bias point was set to $V_{GS} = -0.2$ V, $V_{DS} = -1.2$ V, as found in [62]. The output conductance g_{ds} on top of the drain current I_D output characteristic is shown in Figure 3a, and the transconductance g_m on top of the I_D transfer curve is shown in Figure 3b.

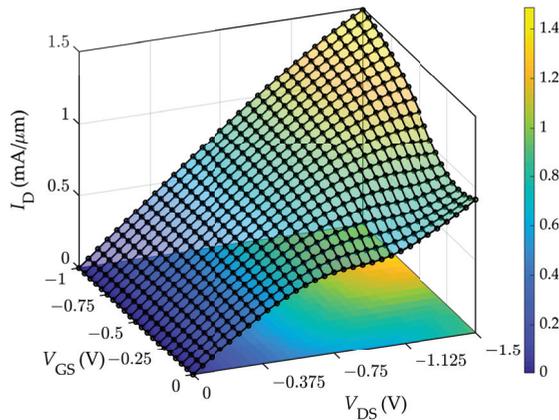


Figure 2. Surface plot of the drain current I_D computed by varying the V_{GS} and V_{DS} .

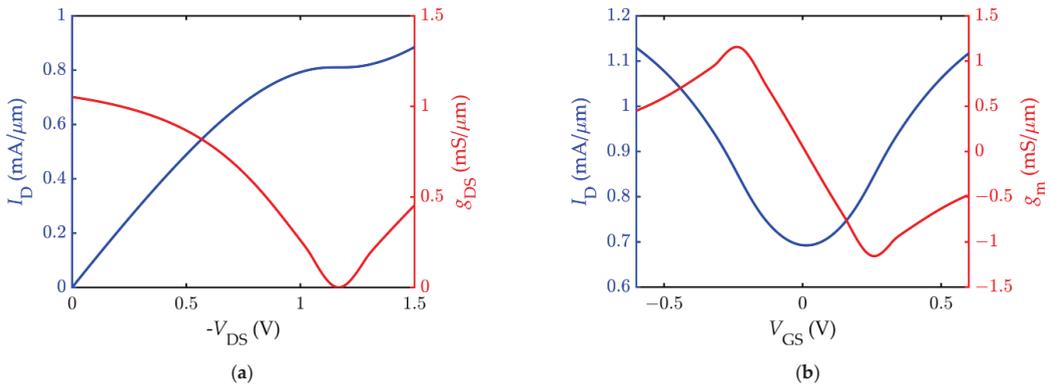


Figure 3. The DC characteristic of the simulated GFET: (a) the drain current I_D (in blue) against the drain-source voltage at $V_{GS} = -0.2$ V, with superimposed output conductance g_{ds} (in red); (b) the drain current I_D (in blue) against the gate-source voltage at $V_{DS} = -1.2$ V, with superimposed transconductance g_m (in red).

2.5. Validation of the Simulated GFET Behaviour

In order to validate the simulation results, the f_T and f_{MAX} obtained by the circuit simulator for the nominal design of the GFET were compared with the measured values reported in [45]. For this purpose, the analysis was performed by biasing the transistor at $V_{GS} = -0.1$ V, $V_{DS} = -1.2$ V, as reported in the paper. In addition, the values computed by means of the small-signal relations reported in Equations (5) and (6) are also reported. As can be observed, the results obtained by using Equations (5) and (6) agree neither with the experiment nor with the simulation, probably due to the nonlinear behaviour of the device and to the model being based on nonreciprocal capacitances. The simulation results replicate the measurements quite well, especially concerning the f_{MAX} , as can be seen in Table 3. Differences between the simulation and the measurement can be caused by the

imperfect value attributed to some of the graphene-related input parameters reported in Table 2, and can be reduced by applying optimization techniques to find the parameters' values that improve the fitting of the measured current curves.

Table 3. Simulated and measured f_T, f_{MAX} at $V_{GS} = -0.1$ V, $V_{DS} = -1.2$ V.

	Simulated	Measured [45]	Computed
f_T (GHz)	9.3	8.2	7.2
f_{MAX} (GHz)	6.1	6.2	4.0

The simulated h_{21} and MAG at the optimal bias point $V_{GS} = -0.2$ V, $V_{DS} = -1.2$ V, instead, return a nominal value for the f_T and f_{MAX} of $f_{T,n} = 29.40$ GHz and $f_{MAX,n} = 14.84$ GHz and are shown in Figure 4.

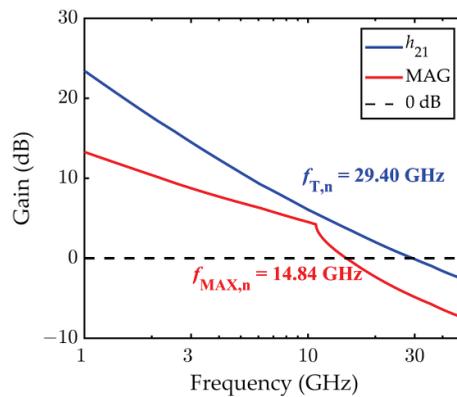


Figure 4. Short-circuit current gain h_{21} and maximum available gain MAG computed in correspondence of the nominal set of input parameters, at the bias point $V_{GS} = -0.2$ V, $V_{DS} = -1.2$ V. The nominal cut-off frequency is $f_{T,n} = 29.40$ GHz, and the nominal maximum oscillation frequency is $f_{MAX,n} = 14.84$ GHz.

3. Tolerance Analysis Results

3.1. f_T Sensitivity

To extract the f_T from the simulation results, the short-circuit current gain h_{21} was computed for the 27 combinations of the input factors, and the scattered data is plotted against the factors in Figure 5a, showing the main effects plot, and against the factor-mixed products in Figure 5b, showing the interaction effects plot. By looking at Figure 5 it can be concluded that the transition frequency f_T is by far more sensitive to the channel length L rather than to the other parameters, as the L factor variation causes the highest location shift of the mean performance, indicated by the blue dots for each level taken by the input factors. This result confirms expectations, since the peak cut-off frequency is reported to have a $1/L$ dependence in FETs with short gate lengths, and a $1/L^2$ dependence in FETs with long gate lengths [16]. The two other factors have the same influence on the f_T , and both are much less effective than L . As can be observed from the f_T main effects and interaction effects values reported in Table 4, the main effect of the channel length L , $ME_3 = -7.11$, is by far the highest contribution to the f_T variability. The interactions between the channel length L and the other two factors (i.e., IE_{13} and IE_{23}) are very similar, and comparable to the main effects of t_{OX} and W , ME_1 , and ME_2 . They are less than 10% of the main effect of the L , meaning that W and t_{OX} and their interactions with L impact the response variability by less than 10% of the impact of L .

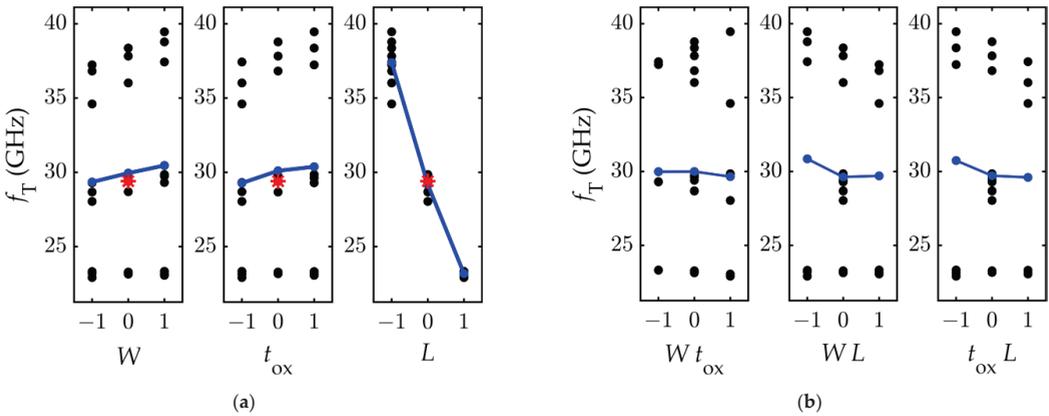


Figure 5. Computed values of f_T against (a) the input factors and (b) the factor-mixed products. The blue lines connect the f_T average values, and the red star marks the response computed at the nominal set of the input parameters.

Table 4. f_T main effects and interaction effects.

	$x_1 (W)$	$x_2 (t_{OX})$	$x_3 (L)$
$x_1 (W)$	ME ₁ = 0.557	IE ₁₂ = -0.166	IE ₁₃ = -0.575
$x_2 (t_{OX})$		ME ₂ = 0.549	IE ₂₃ = -0.570
$x_3 (L)$			ME ₃ = -7.11

Concerning the linearity of the response, the f_T variation induced by the variation of the factors of 10% is approximately linear; in fact, the blue line connecting the average f_T computed at the different levels of the input factors is pretty straight, and closely passes the nominal response $f_{T,n}$.

To account for the slight nonlinearity of the response variable in the regression model, the interaction effects shown in Figure 5b can be considered. The interaction effects are computed by calculating the slope of the line connecting the average values of f_T computed when the product of the coded factors equals -1 and +1. The introduction of such effects can model the small curvatures in the response.

On this basis, the f_T variability can be modelled by:

$$f_T = 29.4 + 0.557 W + 0.549 t_{OX} - 7.11 L - 0.166 W t_{OX} - 0.575 W L - 0.57 t_{OX} L \quad (7)$$

where W , t_{OX} , and L are varying between -1 and +1, following the coding reported in Table 1.

3.2. f_{MAX} Sensitivity

The f_{MAX} variation in response to the variation of the input factors is shown in Figure 6a,b, which report the main effects plot and the interaction effect plot, respectively. As in the previous case, the blue lines connect the f_{MAX} average values computed in correspondence of each level of the factors, and the red star indicates the nominal response $f_{MAX,n}$.

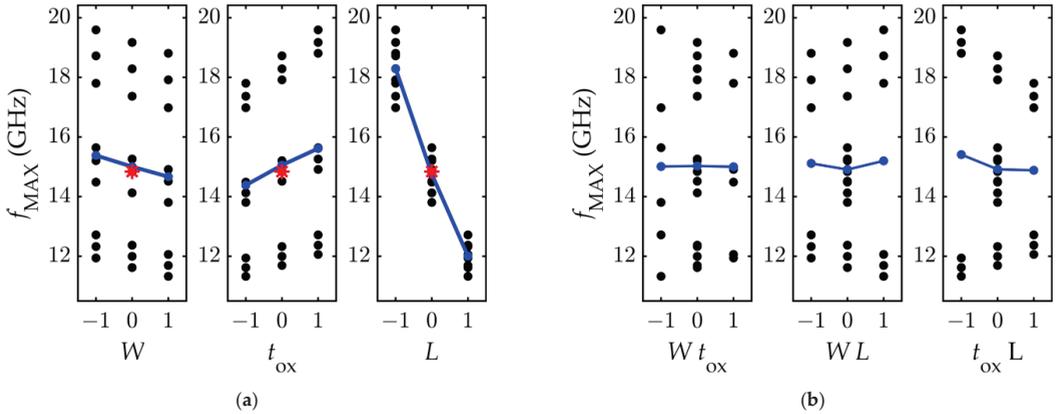


Figure 6. Computed values of f_{MAX} against (a) the input factors and (b) the factor-mixed products. The blue lines connect the f_{MAX} average values, and the red star marks the response computed at the nominal set of the input parameters.

By looking at Figure 6, it can be observed that the factor most influential on the f_{MAX} is, as for the f_T , the channel length L . However, contrarily to what was observed for f_T , the increase of the channel width W causes a decrease of the f_{MAX} . Another noticeable result is that, in this case, the response dependence on the three factors is very linear. In fact, the plots in Figure 6b show that there is no interaction between W and t_{OX} , and that the interaction between W and L is one order of magnitude smaller than the lowest main effect. Moreover, while for the f_T the factors W and t_{OX} had a similar impact on the response, for the f_{MAX} it is observed that the t_{OX} is the second most influential parameter, as its main effect doubles the main effect of W , and is $\approx 20\%$ the main effect of L . This is clearer by observing the computed values of the main effects and interaction effects reported in Table 5.

Table 5. f_{MAX} main effects and interaction effects.

	$x_1 (W)$	$x_2 (t_{OX})$	$x_3 (L)$
$x_1 (W)$	ME ₁ = 0.356	IE ₁₂ \approx 0	IE ₁₃ = 0.042
$x_2 (t_{OX})$		ME ₂ = 0.615	IE ₂₃ = -0.263
$x_3 (L)$			ME ₃ = -3.14

These values allow extracting the linear regression model representing the variability of the PF f_{MAX} , which is:

$$f_{MAX} = 14.84 - 0.356 W + 0.615 t_{OX} - 3.14 L + 0.042 W L - 0.263 t_{OX} L \quad (8)$$

4. Conclusions

An analysis of the impact on the fabrication-related tolerances of the GFET geometrical parameters was performed by means of designed circuit simulations.

The factor variation most influential on the transition frequency and the maximum oscillation frequency uniformity for a GFET-based common-source amplifier is the channel length L , coherently with the concept that the transistor high-frequency limit is inversely proportional to the time the carriers need to cross the channel. Reducing the channel length has great benefits on the transition frequency improvement and helps to improve the maximum frequency, too. Hence, being able to control the channel length reliably and applying all the possible measures to limit the occurrence of any uncontrollable phenomenon interfering with the channel length accuracy is the best way to reduce unwanted fluctuations of the fabricated transistors' cut-off frequency, and therefore improve the intra-

wafer and inter-wafer performance uniformity. The improvement provided by increasing the accuracy of the other geometrical parameters, instead, is very limited. In fact, this analysis has shown that the impact of the channel width W and the top oxide thickness t_{OX} on the f_T is the same, and it is less than 10% of the impact of the channel length L . The interaction between L and the other two factors has an impact comparable to the W and t_{OX} main effect, and must therefore be included in the regression model for the f_T . Concerning the f_{MAX} , the t_{OX} is the second most influential factor, with the main effect that is about 20% of the L main effect. The W impacts on the f_{MAX} by less than 10% the impact of the L . A first-order regression model accounting for interaction between the factors is provided for both the considered performance indicators, allowing both the prediction of the expected variability when the tolerance of process parameters is known, and the definition of a region of acceptability for the factors' tolerances when the variability of the observed performance is constrained.

In conclusion, the reduction of the variability of W and t_{OX} would improve the uniformity of the f_T and f_{MAX} far less than a reduction of the variability of L by an equal percentage amount. The quantitative evaluation of this improvement can be done by using the provided mathematical relations between the quantities of interest. These considerations can support the cost/benefit analysis for the planning of investments to improve the ability of the manufacturing process to control the geometric parameters.

Further work includes the tolerance analysis of different GFET devices found in the literature, in order to compare the robustness of different device layouts and different processes to the fabrication-related tolerances. Moreover, the impact of graphene quality on the RF performance could be assessed quantitatively, providing the model with different inputs depending on the graphene quality indicators.

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Article

Lower Limits of Contact Resistance in Phosphorene Nanodevices with Edge Contacts

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Abstract: Edge contacts are promising for improving carrier injection and contact resistance in devices based on two-dimensional (2D) materials, among which monolayer black phosphorus (BP), or phosphorene, is especially attractive for device applications. Cutting BP into phosphorene nanoribbons (PNRs) widens the design space for BP devices and enables high-density device integration. However, little is known about contact resistance (R_C) in PNRs with edge contacts, although R_C is the main performance limiter for 2D material devices. Atomistic quantum transport simulations are employed to explore the impact of attaching metal edge contacts (MECs) on the electronic and transport properties and contact resistance of PNRs. We demonstrate that PNR length downscaling increases R_C to 192 $\Omega \mu\text{m}$ in 5.2 nm-long PNRs due to strong metallization effects, while width downscaling decreases the R_C to 19 $\Omega \mu\text{m}$ in 0.5 nm-wide PNRs. These findings illustrate the limitations on PNR downscaling and reveal opportunities in the minimization of R_C by device sizing. Moreover, we prove the existence of optimum metals for edge contacts in terms of minimum metallization effects that further decrease R_C by $\sim 30\%$, resulting in lower intrinsic quantum limits to R_C of $\sim 90 \Omega \mu\text{m}$ in phosphorene and $\sim 14 \Omega \mu\text{m}$ in ultra-narrow PNRs.

Keywords: phosphorene; black phosphorus; nanoribbon; edge contact; contact resistance; quantum transport; NEGF; metallization; broadening

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1. Introduction

Two-dimensional (2D) materials are considered to be feasible candidates for future post-silicon electron devices due to their atomic thickness and exceptional mechanical, electronic, and carrier transport properties [1–5]. Among monoelemental 2D materials, monolayer black phosphorus (BP) or phosphorene is frequently identified as promising for future nanoscale field-effect transistors (FETs) due to its acceptable bandgap and carrier mobility that should enable appropriate switching and current-driving performance of phosphorene-based electron devices [6,7]. Recently, experimental demonstration and characterization results have been reported for micro-scale BP FETs [7–9], while theoretical and numerical simulation reports have been published for short-channel and wide-gate phosphorene FETs [4,10,11]. However, phosphorene nanoribbons (PNRs) that are quasi-one-dimensional phosphorene nanostructures are less explored, despite the opportunity provided by quantum confinement to adjust the material and device properties [12–16]. An additional motivation for further research on PNRs is provided by recent reports on fabricated and characterized ultra-narrow PNRs with the widths down to $\sim 0.5 \text{ nm}$ [17,18].

While 2D materials and their nanostructures seem promising for nanodevices, they suffer from high contact resistance (R_C), which limits their performance and conceals their exceptional transport properties. For micro-scale BP FETs, R_C was measured in the range from $\approx 1750 \Omega \mu\text{m}$ [19] and $\approx 1100 \Omega \mu\text{m}$ [9], over $\approx 700 \Omega \mu\text{m}$ [20], down to $\approx 400 \Omega \mu\text{m}$ [21] and $310 \Omega \mu\text{m}$ [22]. Even the best reported R_C values are unacceptably high for transistors in future high-density integrated circuits and, additionally, very little is known about R_C levels

and its behavior in PNR-based devices [23]. The most promising avenue toward low R_C in 2D material-based devices seems to be the concept of edge contacts, i.e., one-dimensional contacts connected only at the edges of the nanostructure. Edge contacts are scalable, not limited by current transfer length as top contacts, and they allow the encapsulation of the 2D material that preserves its exceptional properties and enables long-term stability [24,25]. Almost all theoretical research on 2D material or nanoribbon-based FETs assumes ideal contacts, which only provides upper limits to device performance since the parasitic contact resistance is completely ignored [4,10,11].

In this work, we explore the contact resistance in PNRs with edge contacts using atomistic quantum transport simulations. We describe the metal electrodes by the wide-band limit model that is capable of reproducing metal-induced broadening and metallization effects. The impact of PNR size downscaling on R_C is analyzed for technologically relevant PNR widths (<5.5 nm) and lengths (<16 nm). We reveal significant metallization effects visible in the deterioration of electronic and transport properties of PNRs, which are especially detrimental for nanoribbon lengths under ~8 nm. Contact resistance decreases with the width downscaling but increases considerably when the length decreases. Surprisingly, we show that even in the two-probe simulation setup there exists the optimum metal-nanoribbon interaction parameter that results in the minimum R_C for a given PNR size. With metal edge contacts, optimum electrode material for PNRs is a more strongly-interacting metal in the case of longer devices, whereas ultra-short nanoribbons with lengths under ~6 nm demand contacts with a weaker interaction strength. Our results indicate that the quantum intrinsic limits of R_C , i.e., minimum achievable R_C , in large-area phosphorene devices could be as low as ~90 $\Omega \mu\text{m}$. Moreover, an even lower R_C of ~14 $\Omega \mu\text{m}$ can be obtained in 0.5 nm-wide PNRs with a careful choice of the electrode material. Our results give an encouraging perspective on the suitability of phosphorene and PNR FETs for future nanoscale electron devices and contribute towards theoretical understanding and practical minimization of contact resistance in nanodevices with edge contacts.

2. Methods

A multi-band tight-binding (TB) model from [26] is used for the construction of armchair PNR Hamiltonians that enter the retarded Green's function within the non-equilibrium Green's function (NEGF) formalism for quantum transport. This TB model agrees well with more advanced GW simulations for electron energies up to ~2 eV away from the Fermi level. While a more advanced Hamiltonian, e.g., one resulting from *ab initio* simulations, would improve the bandstructure accuracy in ultra-narrow PNRs [16], we choose a simpler model to reduce the computational burden since we investigate numerous devices of different sizes and contact-device interaction strengths. Regarding device size, we focus on technologically relevant extremely-scaled PNRs with the widths (W) under ~5.5 nm and lengths (L) below ~16 nm. The largest PNR under study consists of 2312 phosphorus atoms, and as many orbitals in the Hamiltonian matrix.

Atomistic NEGF calculations are employed to investigate the electronic and transport properties of ultra-scaled PNRs, and to calculate contact resistance that emerges in PNRs after attaching metal edge contacts (MECs). Ballistic transport simulations are carried out by assuming a two-probe configuration, i.e., two MECs attached on the left and right edge of the nanoribbon, as illustrated in Figure 1. The NEGF formalism solves the Schrödinger's equation for a given system with open boundary conditions (OBCs) [27,28]. The retarded Green's function of the device is given by:

$$G^R(E) = \left[(E + i0^+)I - H - \Sigma_1^R(E) - \Sigma_2^R(E) \right]^{-1} \quad (1)$$

where E is the energy, I is the identity matrix, H is the device Hamiltonian, and Σ matrices are the retarded contact self-energies that account for OBCs in the nanoribbon imposed by the two attached MECs (left contact or contact 1, and right contact or contact 2). Our

existing NEGF code, written in C/C++ and Compute Unified Device Architecture (CUDA) for heterogeneous CPU-GPU execution, and previously demonstrated on graphene, silicene, germanene and phosphorene nanostructures [29,30], is used for calculations in this work.

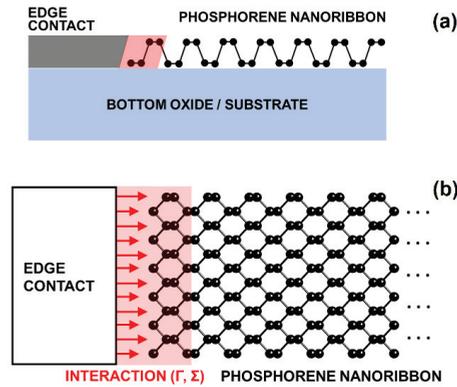


Figure 1. (a) Side-view and (b) top-view of the left metal edge contact attached to the PNR. Light red shaded area indicates the extent of metal-nanoribbon interaction across the closest super-cell, described by the broadening parameter (Γ) or contact-self energy (Σ).

Regarding the OBCs, we study the impact of attaching ideal and metal edge contacts on the electronic and transport properties of PNRs. The ideal edge contacts (IECs) are semi-infinite regions with the same geometry and bandstructure as the central region. Setting IECs in NEGF simulations is common throughout the literature, and this approach eliminates destructive interference at contact-device interfaces and results in perfect step-like transmission functions. In this work, MECs are treated with the wide-band limit (WBL) model in which only the constant imaginary part of contact self-energy matrices is retained [28]. As shown previously in the case of GNRs [31], we set the initial value of the nanoribbon-MEC interaction strength to $-\text{Im}\Sigma^R = 0.9$ eV, in accordance with the average hopping parameter in the TB model for phosphorene, and with the expected density of states (DOS) in the model metal near the Fermi level [28,31]. We analyze the effects of changing $-\text{Im}\Sigma^R$ from the initial to lower and higher values, thus exploring the consequences of attaching weakly and strongly-interacting metals to the PNR, respectively. The MECs are assumed to be Ohmic so tunnel or Schottky barriers are disregarded to solely study the impact of metal-induced broadening or metallization effects. We note that our approach could be applied to large top contacts as well, but contact and device sizes are limited by the available computational facilities since atomistic NEGF simulations are very computationally intensive.

After transmission is calculated from the retarded Green's function [32], we find the PNR conductance at 300 K from the expression:

$$G = \frac{2e^2}{h} \int_0^\infty T(E) (-\partial f(E - E_F) / \partial E) dE, \quad (2)$$

where $T(E)$ is the transmission function, $f(E - E_F)$ is the Fermi-Dirac distribution function, E_F is the Fermi level set to 50 meV away from the conduction band minimum, e is the electronic charge, and h is the Planck's constant. Attaching WBL contacts induces broadening and decreases the transmission and conductance in the conduction and valence bands [31,33]. Therefore, by comparing the conductance values between the IEC and MEC cases, we can calculate the added contact resistance introduced by edge metal contacts using

$$R_C = \frac{1}{G_{MEC}} - \frac{1}{G_{IEC}}, \quad (3)$$

where G_{MEC} and G_{IEC} are PNR conductances with either metal or ideal edge contacts, respectively.

3. Results and Discussion

First, we focus on investigating the impact of PNR width downscaling from 5.4 nm to 0.5 nm on the electronic and transport properties of PNRs with IECs and MECs. Figure 2a shows the DOS in 2.5 nm-wide PNRs and we observe oscillations in DOS in the case of MECs, in contrast to van Hove singularities obtained for ideal contacts. These oscillations are known to occur in graphene and other nanodevices with metallic contacts [34], and can be easily understood from an analytical solution for a one-dimensional atomic chain. For the atomic chain, electron dispersion can be found to be $E(k) = E_0 + 2t\cos(ka)$, where k is the wave-vector or crystal momentum, E_0 is the local orbital energy, t is the hopping parameter, and a is the distance between atoms in the chain. Setting $\Sigma_1 = \Sigma_2 = -i\Gamma/2$ for the MEC case, where Γ is the broadening parameter, and using Equation (1) for the Green's function, we analytically obtain the following spectral function:

$$A(E) = G^R(\Gamma_1 + \Gamma_2)G^A = \frac{2\Gamma}{(E - E_0)^2 + \Gamma^2} \quad (4)$$

where G^A is the advanced Green's function. Therefore, $A(E)$ and density of states defined as $DOS(E) = A(E)/\pi$ are clearly Lorentzian curves centered at E_0 , i.e., at band center, that decrease towards band edges. This characteristic is in stark contrast to the case of ideal contacts that exhibits singularities at band edges and minimum DOS at the band center in 1D structures [27].

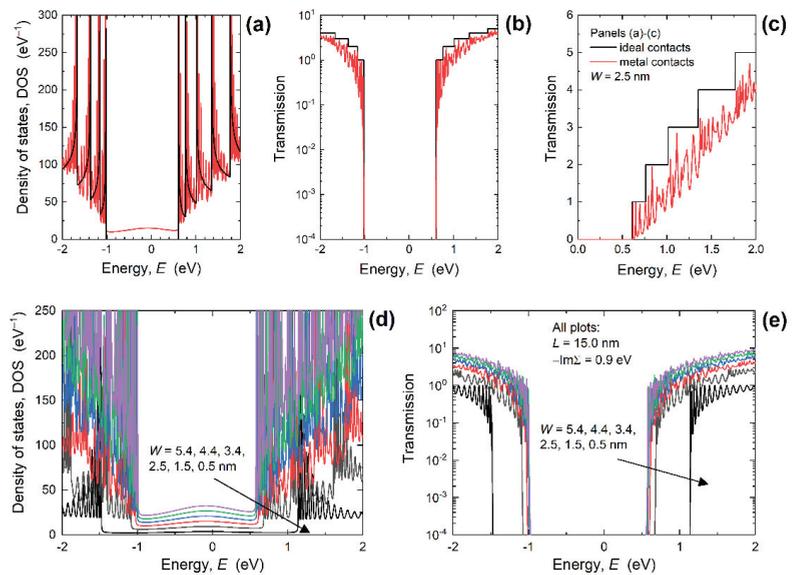


Figure 2. (a) DOS in linear, and transmission in (b) logarithmic and (c) linear scale for 15 nm-long and 2.5 nm-wide PNRs with ideal and metal edge contacts. Impact of width scaling on (d) DOS and (e) transmission in 15 nm-long PNRs with MECs. For all MEC-PNRs, $-\text{Im}\Sigma^R = 0.9$ eV.

The impact of attaching MECs is also visible in the appearance of metal-induced gap states (MIGS) between the valence band maximum (VBM) and conduction band minimum (CBM). However, these states are clearly strongly localized as can be seen in Figure 2b that reports the transmission through the 2.5 nm-wide PNR with IECs and MECs.

The transmission is extremely low inside the bandgap so the transport gap (E_{TG}) exists. Therefore, MIGS do not contribute to transport, which is beneficial for FETs that need a transport gap to achieve efficient switching between the ON and OFF states. These findings demonstrate that PNRs are a more plausible solution of ultra-scaled FETs than GNRs given the considerable metallization-induced E_{TG} decrease reported for GNRs with MECs [31]. While the energy gap of PNRs is immune to MEC-induced metallization effects, the characteristic shown in linear scale in Figure 2c demonstrates a significant transmission suppression by MECs. Lorentzian oscillations are also reported in the transmission as in the DOS curves, and the reasons are given in the Supplementary Materials—Supplementary Note S1. In contrast to ideal contacts that result in unitary transmission probability for each conducting mode and a step-like transmission function, attaching MECs described within the WBL model allows destructive interference for electron waves injected from the contact into the nanoribbon [31,33,34].

Figure 2d,e plots the DOS and transmission, respectively, for MEC PNRs with $L = 15$ nm and for various widths. When W decreases from 5.4 nm to 0.5 nm, the MIGS decrease in intensity due to shorter edge contacts in narrower nanoribbons. At the same time, reducing W increases the transport gap of PNRs, with Lorentzian oscillations existing in the transmission functions for all PNRs irrespective of the width. Therefore, in PNR nanodevices with MECs we expect a considerable deterioration of the current driving capabilities, even in the ballistic transport case that presents an upper intrinsic limit to device performance. Assessing device performance is beyond the scope of this work, but the presented data allows the calculation of relevant conductance values and enables the extraction of R_C introduced by MECs, as described in Section 2.

The influence of decreasing nanoribbon width on the conductance calculated for $E_F = \text{CBM} + 50$ meV at 300 K is reported in Figure 3a for 15 nm-long PNRs. The conductance deteriorates in narrower devices due to lower transmission (see Figure 2e), which itself is a consequence of a lower number of modes or bands in narrower PNRs. In the case of IECs, the conductance decreases from 1.64 (constant $2e^2/h$ is omitted for clarity) to 0.87 in the examined W range, whereas the conductance drops from 0.43 to 0.24 when MECs are connected to the PNRs. Comparing the two edge contact cases, we find that the conductance deterioration with MECs equals 74% for $W = 5.4$ nm and 72% in 0.5 nm-wide PNRs. Using Equation (3), we extract the contact resistance introduced by MECs and plot R_C versus PNR width in Figure 3b. As the width decreases, R_C increases from 22 k Ω ($W = 5.4$ nm) to 38.3 k Ω ($W = 0.5$ nm), which demonstrates that the narrower PNRs are more susceptible to MEC-induced metallization effects through the transmission deterioration. Figure 3c depicts the width-dependence of the width-normalized R_C , i.e., $R_C W$, which is a common contact resistance figure of merit for electron devices. In contrast to R_C behavior in Figure 3b, $R_C W$ monotonically decreases with the downscaling of nanoribbon width, from 119 $\Omega \mu\text{m}$ for $W = 5.4$ nm down to 19 $\Omega \mu\text{m}$ for $W = 0.5$ nm.

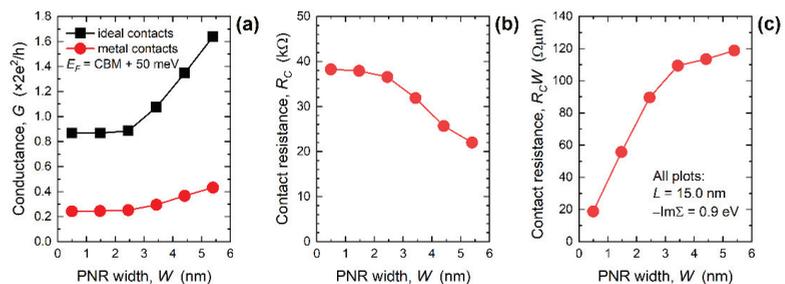


Figure 3. Width-dependence of (a) conductance, (b) contact resistance, and (c) width-normalized contact resistance in 15 nm-long PNRs. For all MEC-PNRs, $-\text{Im}\Sigma^R = 0.9$ eV.

In comparison to GNRs [31], phosphorene nanodevices exhibit a 62% higher R_C for the widest nanoribbons, whereas the narrowest PNRs offer a 10% lower R_C (at $W \sim 0.5$ nm). By extrapolating the results for wide nanoribbons to large-area 2D material devices, our results indicate that micro-scale phosphorene devices should have a significantly higher R_C than graphene devices. This finding agrees with the literature that reports the best R_C of $400 \Omega \mu\text{m}$ [21] to $310 \Omega \mu\text{m}$ [22] for phosphorene FETs, whereas the best reported R_C for graphene FETs is $\sim 80 \Omega \mu\text{m}$ [35]. On the other hand, R_C is very low in narrowest PNRs which means that patterning phosphorene into nanoribbons offers a promising avenue for R_C minimization in ultra-scaled devices that enable high-density integration. The best reported experimental R_C for phosphorene devices is $\sim 300 \Omega \mu\text{m}$, so the space for improvement of the contact resistance exists and is quite extensive since the quantum limit of $R_C W$ reported above ($\sim 20 \Omega \mu\text{m}$) is more than $15\times$ lower than the best-reported measured $R_C W$ value.

Width scaling provides an opportunity to expand the design space through confinement effects, however, length scaling is also important because in modern CMOS industry the channel length decrease is the main driving force behind FET performance improvement. Hence, in the following paragraphs we set a common $W = 3.4$ nm and analyze the electronic and transport properties, and R_C for PNRs with the lengths from ~ 16 nm down to ~ 5 nm. Figure 4a shows the DOS of MEC-PNRs for various lengths with a zoomed-in energy range around the CBM reported in Figure 4b. The DOS again exhibits Lorentzians instead of van Hove singularities due to metallization effects. In the case of L scaling, MIGS are present but the magnitude of localized states inside the bandgap does not change with PNR length. In contrast, Figure 4b shows that DOS inside the conduction band changes considerably when L decreases, with the first DOS peak closest to CBM being shifted away from the CBM when the PNR length is scaled down. The CBM is positioned at $E = 583$ meV in the case of IECs, whereas the closest Lorentzian peak is situated at $E = 595$ meV for $L = 15.9$ nm in PNRs with MECs. Decreasing the length to 7.9 nm moves the first peak to $E = 623$ meV, while for $L = 5.2$ nm the first peak is positioned at $E = 677$ meV, i.e., shifted by 94 meV from the CBM. In addition to significant qualitative changes, we observe that DOS values decrease when L is scaled down, which is expected to decrease the ability of ultra-short PNRs to generate enough charge carriers for acceptable performance of PNR-based FETs.

As reported in Figure 4c, the transmission curves exhibit variations similar to those seen in the DOS. Decreasing L reduces the number of Lorentzians and shifts the first peak away from the CBM. The transmission is greatly reduced in PNRs with MECs, which is especially evident for $L = 5.2$ nm for which the transmission is almost completely suppressed in the entire energy range corresponding to the first transmission step of the PNR with IECs. Results presented in Figure 4c seem to indicate that the downscaling of the length of PNRs with MECs leads to the increase of the transmission gap, but Figure 4d that reports the transmission in logarithmic scale reveals a more complicated picture. Namely, while the transmission decreases with L downscaling in the energy range above the CBM, the opposite is true inside the bandgap. As the PNR length decreases, transmission probability below the CBM increases considerably, which leads to the contraction of the transport gap. If we define the transport gap as the energy range where the transmission is lower than 0.001 , we find that E_{TG} decreases by 56 meV when $L = 7.9$ nm and by 252 meV in the 5.2 nm-long PNR. Since the existence and value of E_{TG} is very important for the practical realization of FETs, this finding clearly shows that broadening or metallization effects must be included into the physical framework used for the simulation of nanoscale electron devices. We have previously reported that in ultra-short GNRs the transport gap closes completely due to these metallization effects [31], but PNRs are evidently more resilient to the influence of metal edge contacts than GNRs since E_{TG} still exists, albeit being somewhat smaller.

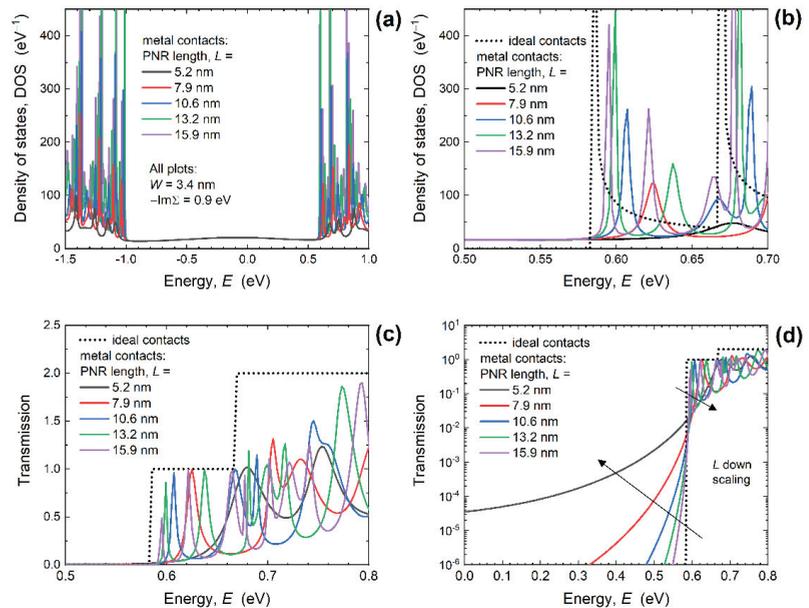


Figure 4. DOS in (a) entire energy range, and (b) in the conduction band for 3.4 nm-wide PNRs of various lengths with ideal and metal edge contacts. Influence of length downscaling on transmission in the (c) linear and (d) logarithmic scale. For all MEC-PNRs, $-\text{Im}\Sigma^R = 0.9$ eV.

The observed strong suppression of transmission near the CBM consequently decreases the conductance and induces contact resistance at the two MEC-nanoribbon interfaces. Figure 5a reports the conductance calculated for $E_F = \text{CBM} + 50$ meV and 300 K versus PNR length for 3.4 nm-wide PNRs with IECs and MECs. While the conductance is length-independent in the case of ideal contacts, it noticeably decreases for $L < 8$ nm when MECs are attached to PNRs. Hence, conductance difference between the two contact configurations is largest in the shortest devices, which is also seen in the extracted R_C shown in Figure 5b. As the length is downscaled, R_C increases from 31.9 k Ω ($L = 15.9$ nm) to 56.6 k Ω ($L = 5.2$ nm), which is a consequence of the greatly decreased transmission near the CBM in 5.2 nm-long PNRs (see Figure 4c). After width-normalization the contact resistance curve in Figure 5c stays qualitatively the same as in Figure 5b. The $R_C W$ equals 109 $\Omega \mu\text{m}$ for $L = 15.9$ nm, stays almost constant down to $L = 7.9$ nm, and then increases to 192 $\Omega \mu\text{m}$ in MEC-PNRs that are only 5.2 nm long. In addition to transport gap decrease, the observed boost of $R_C W$ is yet another negative consequence of attaching metal contacts if we consider ultra-scaled PNRs as channel material for future FETs.

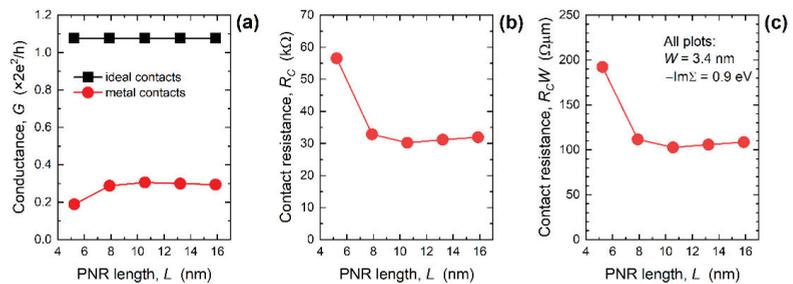


Figure 5. Length-dependence of (a) conductance, (b) contact resistance, and (c) width-normalized contact resistance in 3.4 nm-wide PNRs. For all MEC-PNRs, $-\text{Im}\Sigma^R = 0.9$ eV.

All the results considered so far are based on using $-\text{Im}\Sigma^R = 0.9$ eV in MEC self-energy matrices, which presents a model metal material with moderately-strong interactions with the nanoribbon. However, we have recently shown for FETs based on various mono-elemental 2D materials that there exists the optimum interaction parameter value leading to the lowest transmission decrease, which enables the minimization of R_C in such nanodevices [23]. An example concerning optimum $-\text{Im}\Sigma^R$ for transmission is given for a 2.45 nm-wide and 15 nm-long PNR in the Supplementary Materials—Supplementary Note S2, Figure S1. This finding is in accordance with the study dealing with reflections and transmissions in atomic chains and carbon nanotubes connected to wide-band leads reported in [36]. An illustrative example based on 1D atomic chains about the evolution of eigenstates and transmission functions, and the existence of the optimum interaction parameter is provided in Supplementary Materials—Supplementary Note S3, Figures S2–S4. For phosphorene FETs with 15 nm-long channels, the optimum $-\text{Im}\Sigma^R$ of ~ 2 eV was reported in [23]. Therefore, it seems reasonable to assume that such optimum interaction parameters will exist also in the case of a two-probe setup assessed in this work with the aim of finding quantum limits of R_C in PNRs with metal edge contacts. In the following discussions, we calculate $R_C W$ for MEC-PNRs of various dimensions, and for $-\text{Im}\Sigma^R$ that ranges from 0.01 eV to 20 eV. The $-\text{Im}\Sigma^R$ value range is chosen according to studies on graphene-metal and carbon nanotube-metal contacts in [37,38]. While we do not perform *ab initio* interface studies for phosphorene-metal systems as in [39–41] due to heavy computational burden of doing so for a large variety of nanoribbon sizes and metal choice, the WBL approach allows us to explore the impact of weakly, moderately and strongly-interacting metal electrodes on the contact resistance in PNR nanodevices. Generally, the low $-\text{Im}\Sigma^R$ values in our approach correspond to weakly interacting metals such as Al, Ag, Au, Cu, and higher $-\text{Im}\Sigma^R$ values describe strongly interacting metals such as Cr, Ni, Pd, Ti, where the interaction strength is assessed in detail by *ab initio* calculations in [39].

Figure 6a reports the dependence of $R_C W$ on the interaction strength in 2.45 nm-wide and 15 nm-long phosphorene nanoribbons. Starting from very weakly interacting metals ($-\text{Im}\Sigma^R = 0.01$ eV) where $R_C W = 11.2$ k $\Omega\mu\text{m}$, the resistance first decreases and reaches a minimum of 61 $\Omega\mu\text{m}$ for the optimum $-\text{Im}\Sigma^R$ of 2 eV, and then increases to 247 $\Omega\mu\text{m}$ when strongly-interacting ($-\text{Im}\Sigma^R = 20$ eV) MECs are attached to the PNR. In comparison to the initial resistance value of 90 $\Omega\mu\text{m}$ for $W = 2.45$ nm in Figure 3c, a careful choice of contact material can reduce $R_C W$ by 32%. Assuming the optimum interaction parameter of 2 eV for all 15 nm-long devices, in Figure 6b, we report $R_C W$ values for the entire examined PNR width range. In this case the resistance decreases from 84 $\Omega\mu\text{m}$ for $W = 5.4$ nm down to 14 $\Omega\mu\text{m}$ in the 0.5 nm-wide MEC-PNR. The improvement is almost constant and equals $\sim 30\%$ for nanoribbon widths down to ~ 1.5 nm, whereas $R_C W$ drops by 23% for 0.5 nm-wide PNRs with MECs and $-\text{Im}\Sigma^R = 2$ eV. The characteristics reported in Figure 6b indicate that a minimum $R_C W$ of ~ 90 $\Omega\mu\text{m}$ is achievable in large-area phosphorene devices with edge contacts, which puts these lower quantum limits of R_C in phosphorene close to the best reported contact resistance in graphene devices [24,35]. In addition, our results show that

the contact resistance can be further minimized to $\sim 14 \Omega \mu\text{m}$ by using ultra-narrow PNRs as channel material in ultra-scaled FETs.

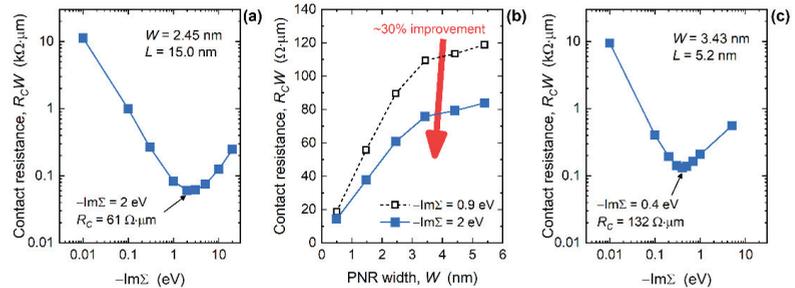


Figure 6. (a) Dependence of width-normalized contact resistance on interaction strength in 2.45 nm-wide and 15 nm-long PNRs with MECs. (b) Impact of PNR width downscaling on $R_C W$ for the two $-\text{Im}\Sigma^R$ values, initial and the optimum one. (c) $R_C W$ versus interaction strength in 3.43 nm-wide and 5.2 nm-long PNRs with MECs.

Concerning the PNR length scaling, optimum $-\text{Im}\Sigma^R$ stays the same down to about $L = 10 \text{ nm}$ (not shown), and then decreases. Figure 6c plots $R_C W$ versus the interaction parameter $-\text{Im}\Sigma^R$ for 3.4 nm-wide PNRs with a length of 5.2 nm. For this device, $R_C W$ starts at 5.5 k $\Omega \mu\text{m}$ in the case of weakly-interacting WBL edge contacts, then decreases and reaches the optimum value of 132 $\Omega \mu\text{m}$ for $-\text{Im}\Sigma^R = 0.4 \text{ eV}$, after which $R_C W$ increases to 559 $\Omega \mu\text{m}$ for the strongest-interacting MECs considered. The improvement of $R_C W$ in 5.2 nm-long PNRs with $-\text{Im}\Sigma^R = 0.4 \text{ eV}$, over the initial case where $-\text{Im}\Sigma^R$ was 0.9 eV, amounts to 31%. Hence, even in the shortest devices, the contact resistance can be significantly reduced despite the very strong metallization-induced effects. Nevertheless, the choice of optimum electrode material changes in shorter devices that clearly benefit from less-interacting MECs (optimum $-\text{Im}\Sigma^R = 0.4 \text{ eV}$) than longer PNRs (optimum $-\text{Im}\Sigma^R = 2 \text{ eV}$) and, by extrapolation, large-area phosphorene devices with edge contacts.

4. Conclusions

Using atomistic quantum transport simulations, we studied the consequences of attaching metal electrodes in the edge-contact configuration on the electronic and transport properties of ultra-scaled PNRs. Since we ignore tunnel and Schottky barriers, our approach allows us to explore upper performance limits and lower limits on contact resistance in these devices. Attaching MECs leads to Lorentzian peaks in the DOS and transmission characteristics, appearance of localized MIGS inside the bandgap, noticeable narrowing of the transport gap, and overall suppression of the transmission in the conduction and valence bands. This suppression decreases the device conductance and introduces additional contact resistance at electrode-nanoribbon interfaces. We have shown that PNR width downscaling in the 5.4–0.5 nm range decreases $R_C W$ from 119 $\Omega \mu\text{m}$ down to 19 $\Omega \mu\text{m}$. Therefore, patterning phosphorene into PNRs provides a compelling way to minimize contact resistance to levels acceptable to the CMOS industry for nanoscale FETs. In contrast to width scaling, $R_C W$ increases with decreasing PNR length from 109 $\Omega \mu\text{m}$ when $L = 15.9 \text{ nm}$ to 192 $\Omega \mu\text{m}$ in 5.2 nm-long PNRs with MECs. In addition to E_{TC} decrease, the boosted $R_C W$ in ultra-short PNRs also limits their feasibility as channel material in ultra-scaled FETs, and emphasizes the importance of including metallization effects in device simulation at this scale. Finally, we have demonstrated the existence of optimum interaction parameters or optimum electrode materials that can significantly improve $R_C W$ (30% in comparison to the initial case of $-\text{Im}\Sigma^R = 0.9 \text{ eV}$). Surprisingly, shorter PNRs favor less-interacting metals (optimum $-\text{Im}\Sigma^R = 0.4 \text{ eV}$), whereas longer PNRs profit from more strongly interacting electrodes (optimum $-\text{Im}\Sigma^R = 2 \text{ eV}$) that reduce $R_C W$ to very low levels, i.e., $\sim 14 \Omega \mu\text{m}$ in the narrowest PNRs. Our work proves that there is enough room

for $R_C W$ improvement in BP and PNR devices since quantum limits of $R_C W$ reported in this work are an order of magnitude lower than the best reported measured contact resistance. Regarding large-area phosphorene devices with edge contacts, we show that $R_C W$ of $\sim 90 \Omega \mu\text{m}$ is achievable, which is close to the best reported contact resistance in graphene devices.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/nano12040656/s1>, pdf document containing additional simulation results, mainly on 1D atomic chains to illustrate the emergence of contact resistance and existence of optimum electrode material in nanodevices with edge contacts: Figure S1: Transmission of 15 nm-long and 2.45 nm-wide PNRs with MECs for various contact self-energy or interaction parameter values ranging from 0.09 eV to 20 eV, Figure S2: Transmission function of a 5-atom chain with ideal and metal contacts for different ratios of the contact self-energy and inter-atomic hopping parameter $-\text{Im}\{\Sigma\}/t$ that ranges from 0.1 to 10, Figure S3: The same as in Figure S2 but for $-\text{Im}\{\Sigma\}/t$ values that range from 0.9 to 1.5, Figure S4: Transmission in a 5-atom chain for weakly and very strongly interacting MECs, and dependence of eigenvalues on the interaction strength.

Author Contributions: Conceptualization, M.P.; methodology, M.P., M.M. and T.Ž.; data curation, M.M., A.Z., T.Ž. and M.P.; writing—original draft preparation, M.P., M.M. and A.Z.; writing—review and editing, M.P.; project administration, M.P.; funding acquisition, M.P. All authors have read and agreed to the published version of the manuscript.

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Article

Electric Transport in Few-Layer ReSe₂ Transistors Modulated by Air Pressure and Light

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Abstract: We report the fabrication and optoelectronic characterization of field-effect transistors (FETs) based on few-layer ReSe₂. The devices show n-type conduction due to the Cr contacts that form low Schottky barriers with the ReSe₂ nanosheet. We show that the optoelectronic performance of these FETs is strongly affected by air pressure, and it undergoes a dramatic increase in conductivity when the pressure is lowered below the atmospheric one. Surface-adsorbed oxygen and water molecules are very effective in doping ReSe₂; hence, FETs based on this two-dimensional (2D) semiconductor can be used as an effective air pressure gauge. Finally, we report negative photoconductivity in the ReSe₂ channel that we attribute to a back-gate-dependent trapping of the photo-excited charges.

Keywords: 2D materials; rhenium; selenides; ReSe₂; field-effect transistor; pressure; negative photoconductivity

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1. Introduction

Rhenium diselenide (ReSe₂) is a member of the layered transition metal dichalcogenides (TMDs), which has attracted a lot of attention due to the extremely anisotropic electrical, optical and mechanical properties stemming from the strong in-plane anisotropy consequence of its reduced crystal symmetry [1–4]. Contrary to other hexagonal TMDs, the room temperature thermodynamically stable 1T phase for ReSe₂ has a distorted triclinic symmetry, which endows the material with anisotropic responses in many properties [5–7].

Monolayer ReSe₂ has an indirect bandgap of 1.34 eV [8–10], reducing to 0.98 eV [6] for bulk ReSe₂ with a weak layer dependency. In general, an increase in the layer thickness causes a reduction in band-gap energy and the loss of electric properties of thick ReSe₂ [11].

ReSe₂ has been employed in various electronic and optoelectronic functional devices in order to study its electrical and optical properties. Yang et al. reported that the mobility of ReSe₂ nanosheets increases when the number of layers decreases and highlighted that the properties of ReSe₂ can be tuned by the number of layers and gas molecule gating, making ReSe₂ a promising material for future functional device applications [11]. Optically biaxial and highly anisotropic Mo-doped ReSe₂ (Mo:ReSe₂) was used to investigate the effects of physisorption of gas molecules on few-layer nanosheet-based photodetectors, reporting different sensitivity to the surrounding environment, prompt photoswitching, and high photoresponsivity [12].

The anisotropic nature of ReSe₂ was revealed by Raman spectroscopy under linearly polarized excitations in a study by Zhang et al., who fabricated top-gate ReSe₂ field-effect transistors (FETs), with a high on/off current ratio and a well-developed current saturation in the current–voltage characteristics at room temperature [7]. They synthesized

ReSe₂ directly onto hexagonal boron nitride (h-BN) substrates to improve the electron and hole mobility and demonstrated that the ReSe₂-based photodetectors exhibit polarization-sensitive photoresponsivity due to the intrinsic linear dichroism, originating from high in-plane optical anisotropy, thus, identifying ReSe₂ as a highly anisotropic two-dimensional (2D) material for novel electronic and optoelectronic applications.

Similarly, a near-infrared ReSe₂ photodetector featuring high photoresponsivity and a short photoresponse time, in the order of 10 ms, was demonstrated by Kim and coworkers, achieving high photo and temporal responses simultaneously by applying a p-doping technique based on hydrochloric acid to a selected ReSe₂ region [13].

Ambipolar FETs were obtained from multi-layer ReSe₂, mechanically exfoliated onto a SiO₂ layer by Pradhan et al., who demonstrated that it is possible to utilize the ambipolarity to fabricate logical elements or digital synthesizers [10]. Similarly, ambipolar all-2D ReSe₂ FET with a h-BN gate dielectric and graphene contacts were investigated by Lee and coworkers, who used the ambipolar transfer characteristics, attributed to the tunable Fermi level of the graphene contact, to demonstrate an inverter in a logic circuit [14].

Corbet et al. proposed a method to improve the contact resistance in few-layer ReSe₂ FETs, by up to three orders of magnitude, using ultra-high-vacuum annealing [15]. A low contact resistance was also obtained in single-layer ReSe₂, encapsulated in h-BN using scandium/gold contacts, and this enabled Khan and coworkers [16] to measure a large field-effect charge carrier mobility and responsivity.

Xing et al. addressed the challenge of the controlled synthesis of high-quality ultrathin ReSe₂, developing an approach for synthesizing 2D ReSe₂ flakes with a thickness down to monolayer by chemical vapor transport, through carefully tuning the growth kinetics [17]. The FETs fabricated with such flakes showed n-type semiconducting behavior with mobility of a few cm² V⁻¹ s⁻¹, comparable to the values measured using mechanically exfoliated flakes.

Polarization-resolved ReSe₂ photodetectors were recently studied by Tian and Liu, who reported a van der Waals heterojunction ReSe₂/WSe₂-based photodetector, with high responsivity and detectivity at room temperature. Remarkably, they demonstrated that the photoresponse of their devices is a function of the polarized angle of the incident light, indicating the effective polarized light detection [18].

Pressure is commonly used to understand the interlayer interaction in layered materials. High-hydrostatic pressures of several kbar were applied to ReSe₂ (and ReS₂) exfoliated flakes and the effect on their optical properties was investigated, finding that the energies of the two main excitonic transitions decrease in energy with increasing pressure [19]. The negative pressure coefficients were attributed to the destabilization of the p_z orbital with increasing pressure, demonstrating that ReSe₂ does not exhibit a strong electronic decoupling and, hence, the optoelectronic properties of few-layered ReSe₂ could be drastically different from the bulk form.

Conversely, the effect of low pressure on ReSe₂ has been rarely investigated in the literature.

In the present study, we fabricate back-gate FETs with a few-layer ReSe₂ channel and study the electric transport from room pressure down to 10⁻⁵ mbar. We find that air pressure has a dramatic effect on the channel conductivity, which increases by more than two orders of magnitude when the pressure decreases. We explain such behavior in terms of the desorption of oxygen and water molecules from the ReSe₂ surface in high vacuum. Importantly, we observe that the effect of air pressure is reversible, highlighting that back-gate ReSe₂ FETs can be exploited as effective pressure gauges. Moreover, we report a reduction of the channel conductivity when the device is illuminated, i.e., a negative photoconductivity, that has not been reported before for ReSe₂. The dependence of the negative photoconductivity on the gate voltage suggests that photo-excited free charge carriers are attracted towards the gate and captured at the interface, with the dielectric layer contributing to the observed loss of conductivity.

2. Materials and Methods

Ultrathin ReSe₂ flakes were exfoliated from bulk ReSe₂ single crystals using a standard mechanical exfoliation method by adhesive tape. The flakes were transferred onto highly doped n-type (resistivity 0.005 Ω cm) silicon substrates, covered by 290 nm thick SiO₂, which serves as a global back gate. Photolithography and standard lift-off process of evaporated Cr/Au (5 nm/100 nm) were applied to define metal contacts. Figure 1a reports the crystal structure and Figure 1b shows the schematic of a ReSe₂ FET with the circuit used to control the Si/SiO₂ back-gate and the source-drain bias on the 2D semiconducting channel. We adopted an interdigitated layout with 4 parallel channels corresponding to a total channel width $W = 26.0 \mu\text{m}$ and length $L = 0.78 \mu\text{m}$. An optical top view of a typical device is shown in Figure 1c. The thickness of the flake was measured by an atomic force microscope (Nanosurf AG, Liestal, Switzerland), obtaining the height profile displayed in Figure 1d that confirms a thickness of 1.84 nm, corresponding to 3 layers [20].

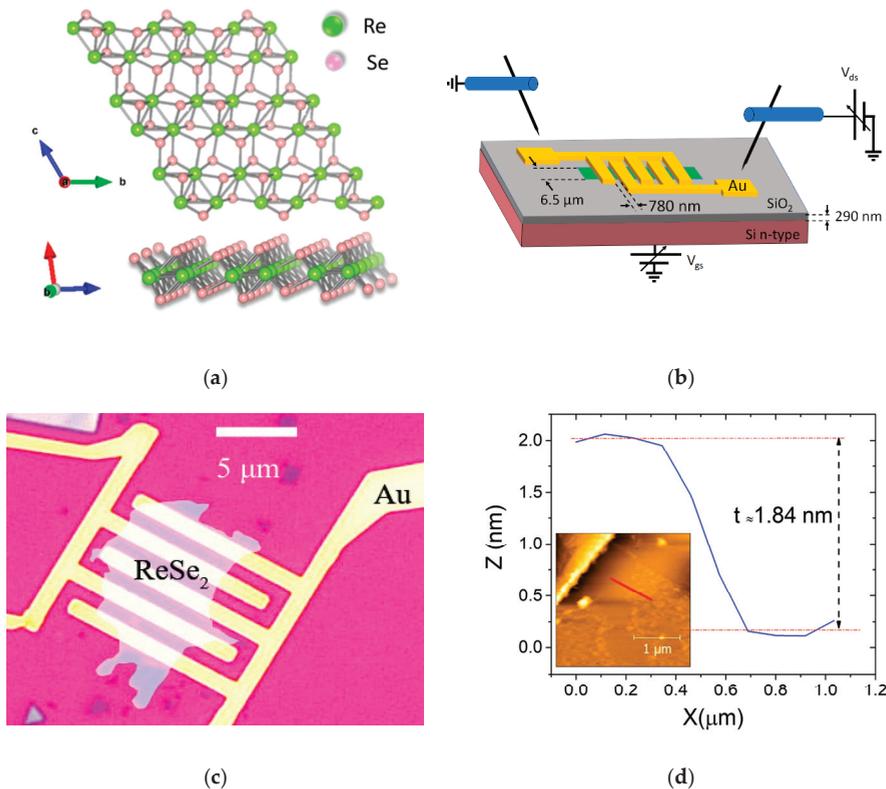


Figure 1. (a) Top view and side view of ReSe₂ atomic structure (the green and pink dots represent the Re and Se atoms, respectively); (b) schematic of the ReSe₂ back-gated FET with interdigitated source/drain leads. (c) Optical image of the ReSe₂ device with interdigitated Cr/Au leads. The flake is highlighted. (d) AFM vertical profile showing the flake thickness of 1.84 nm.

Electric measurements were carried out in two-probe configuration in a Janis ST-500 Probe Station (Lake Shore Cryotronics, Inc., Westerville, OH, USA) equipped with nanoprobe connected to the source/drain leads (Figure 1b). The back-gate voltage was applied through the sample holder of the probe station which was in direct electrical contact to the Ag-pasted n-Si substrate. The measurements were performed by the source-measurement units of a semiconductor characterization system Keithley 4200 SCS (Tek-

tronix, Inc., Beaverton, OR, USA), with current and voltage sensitivity better than 1 pA and 2 μ V, respectively. For the transistor characterization, the source was grounded while the drain (V_{ds}) and gate (V_{gs}) voltages were either swept or stepped while the drain (I_d) and gate (I_g) currents were monitored. The measured gate leakage current was always < 10 pA, confirming the integrity of the SiO₂ gate dielectric.

The electric measurements were performed at controlled air pressure, from room pressure to 10^{-5} mbar. Under the combined action of a rotatory and a turbomolecular pump connected in series to a probe station and a valve system, it was possible to control the pressure stepwise. The pressure was monitored through the pressure gauge TPG261 (Pfeiffer, Asslar, Deutschland). The photoresponse of the device was investigated using an array of 144 white LEDs with a spectrum ranging from 400 to 750 nm and peaks at 450 nm and 540 nm, a color temperature of 6000 K, and with 1 mW/cm² intensity.

3. Results and Discussion

Initially, the ReSe₂ transistor was characterized in dark and at room temperature and pressure, followed by investigating the effect of the lowering pressure in the same conditions of temperature and darkness. Finally, we explored the photoresponse of the fabricated device.

3.1. Transistor Characterization

Figure 2a,b report the output ($I_d - V_{ds}$ at fixed V_{gs}) and transfer ($I_d - V_{gs}$ at fixed V_{ds}) characteristics of the fabricated ReSe₂ FET, respectively. We limited the drain bias to 3 V and gate voltage range to ± 30 V to prevent damage to the device and, in particular, to the SiO₂ gate dielectric. The $I_d - V_{ds}$ curves (Figure 2a) show that the drain current is modulated by the gate voltage V_{gs} and stays below 10 pA for negative V_{gs} but increases abruptly for positive V_{gs} . This behavior is typical of a n-type transistor [21,22]. Furthermore, for all gate voltages, the $I_d - V_{ds}$ curves are asymmetric, with slightly higher current at positive V_{ds} , pointing to the formation of low Schottky barriers at the ReSe₂/Cr/Au contacts [23–26]. The presence of a Schottky barrier is confirmed also by the limited current that reaches the maximum of 20 nA at $V_{ds} = 3$ V.

The $I_d - V_{gs}$ transfer curves of Figure 2b, shown on both the linear and logarithmic scale, confirm the n-type behavior of the transistor, with off-state at $V_{gs} < 20$ V and on-state for $V_{gs} > 20$ V. The curve on the logarithmic scale shows an on/off current ratio higher than two orders of magnitude and a modest subthreshold swing $SS \simeq 2.8$ V/decade, typical of back-gate 2D transistors with limited gate efficiency and high interface defect density [27–30]. The smooth rise of I_d at negative V_{gs} indicates the appearance of a hole-type conduction. The carrier type can be controlled via the metal contacts. Dominant n-type behavior is obtained in ReSe₂ transistors with low-work-function metal contacts, such as Al or Ti, whose Fermi level aligns above the conduction band minimum of ReSe₂ [7,14,31]. As the conduction band minimum of ReSe₂ is around of 4.5 eV and the valence band maximum is around 5.6 eV [31], the Fermi levels of Cr and Au that have work functions of 4.5 and 5.1 eV, respectively, align within the ReSe₂ bandgap and can favor ambipolar conduction.

The transfer curve on the linear scale is used to estimate the field-effect mobility, μ_{FE} , in the on-state of the transistor for $V_{gs} > 20$ V. The mobility, evaluated as $\mu_{FE} = \frac{L}{W} \frac{1}{C_{ox} V_{ds}} \frac{dI_{ds}}{dV_{gs}}$ (here $C_{ox} = 1.15 \times 10^{-8}$ F cm⁻² is the gate dielectric capacitance per unit area), results $\mu_{FE} \simeq 0.03$ cm² V⁻¹ s⁻¹ slightly lower than the $\mu_{FE} \sim 0.1 - 10$ cm² V⁻¹ s⁻¹, typically measured in few-layer ReSe₂ FETs [5,7,10,11]. We also note that an increase in layer thickness causes a loss of electric properties in ReSe₂ and, in particular, that few-layer ReSe₂ exhibits lower mobility of two orders of magnitude or more than single-layer ReSe₂ [11]. Furthermore, the presence of a Schottky barrier at the contacts [32,33], as well as intrinsic defects in the material and impurities located at the interface with the SiO₂ layer or adsorbates on top of the channel from air exposure during the fabrication and the measurement process [10,34,35], acting as scattering or trapping centers, can contribute to decrease the mobility.

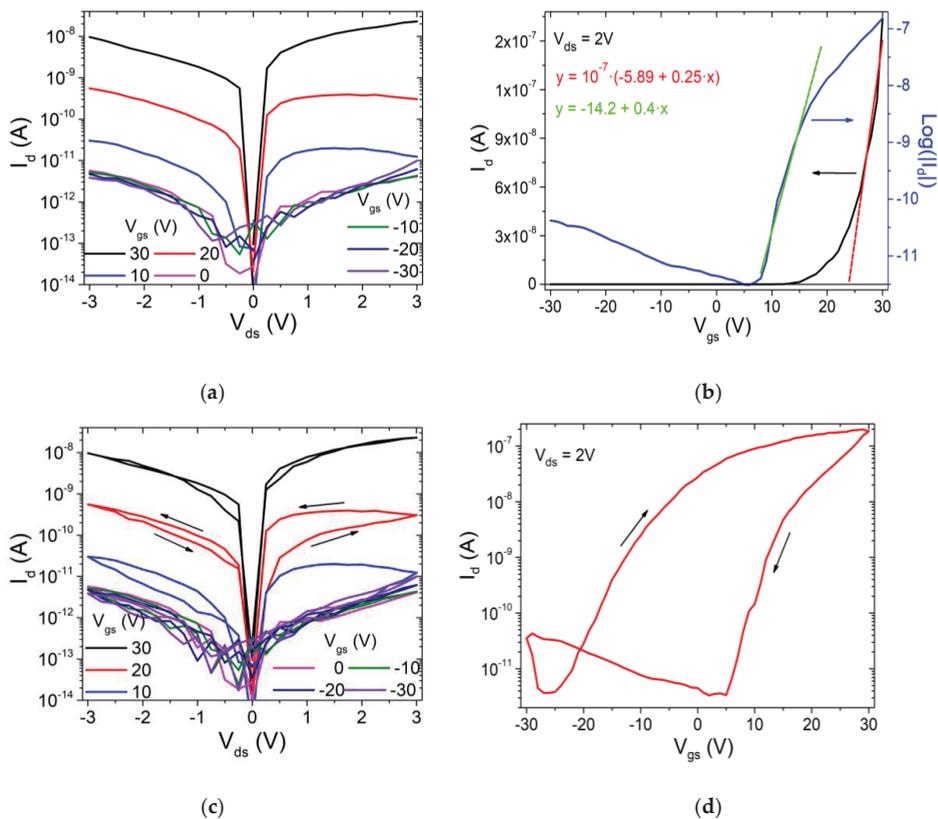


Figure 2. Electrical measurements at normal atmospheric pressure: (a) Output curves for reverse V_{ds} sweep (single). (b) Transfer curve on linear (black) and logarithmic (blue) scale. (c) Output curves for forward and reverse V_{ds} sweeps. (d) Transfer curves for forward and reverse V_{gs} sweeps, showing a wide hysteresis.

The x-axis intercept of the straight line that fits the transfer curve on the linear scale in Figure 2b is assumed as the threshold voltage V_{th} of the transistor and is about 20 V, indicating a n-type enhancement mode device.

More insights in the electric transport through the ReSe_2 channel can be gained from Figure 2c,d, which display a hysteresis on both the output and transfer curves when V_{ds} or V_{gs} are swept in a loop (the forward and reverse sweeps yield different curves). The presence of large hysteresis in the $I_d - V_{ds}$ characteristics has been reported before in monolayer MoS_2 devices, where it was attributed to the multigrain structure of the material and exploited to enable resistive switching devices. The presence of grain boundaries provides the opportunity to fabricate memristors, owing to the phenomenon of migration of defects, such as sulphur vacancies at grain boundaries, by applying a high electric field [36]. The hysteretic behavior in Figure 2c points to a defective ReSe_2 channel, possibly with Se vacancies, consistent with the n-type intrinsic doping and the low mobility. The presence of intrinsic and interfacial defects is confirmed by the huge hysteresis observed in the transfer curve in Figure 2d. Hysteresis in the transfer characteristic is very common in 2D-material-based transistors and has been widely studied and attributed to charge trapping inside the channel material, interface trap states or surface adsorbates [37,38]. The interaction with the SiO_2 dielectric, i.e., the $\text{ReSe}_2/\text{SiO}_2$ interface, is of paramount importance. Indeed, the substitution of the SiO_2 layer by a high-quality h-BN-insulating

substrate, which is atomically flat and free of charge trapping sites, has been shown to result in a strong mitigation of the hysteresis [39].

3.2. Pressure Behavior

To investigate the effect of air pressure on the ReSe₂ channel conductivity, we performed an electric transport measurement, lowering the atmospheric pressure down to 10⁻⁵ mbar. The measurements were performed after keeping the device at the given pressure for several hours to achieve a steady state. Figure 3a shows the output characteristics at three different pressures (room pressure, 3 mbar and 8 × 10⁻⁵ mbar) for increasing gate voltages, ranging from 0 V to 30 V, with steps of 10 V. It can be observed that the channel current increases at lower pressure while the hysteresis decreases, and the asymmetric behavior is unchanged. The reduced hysteresis indicates that surface adsorbates play an important role.

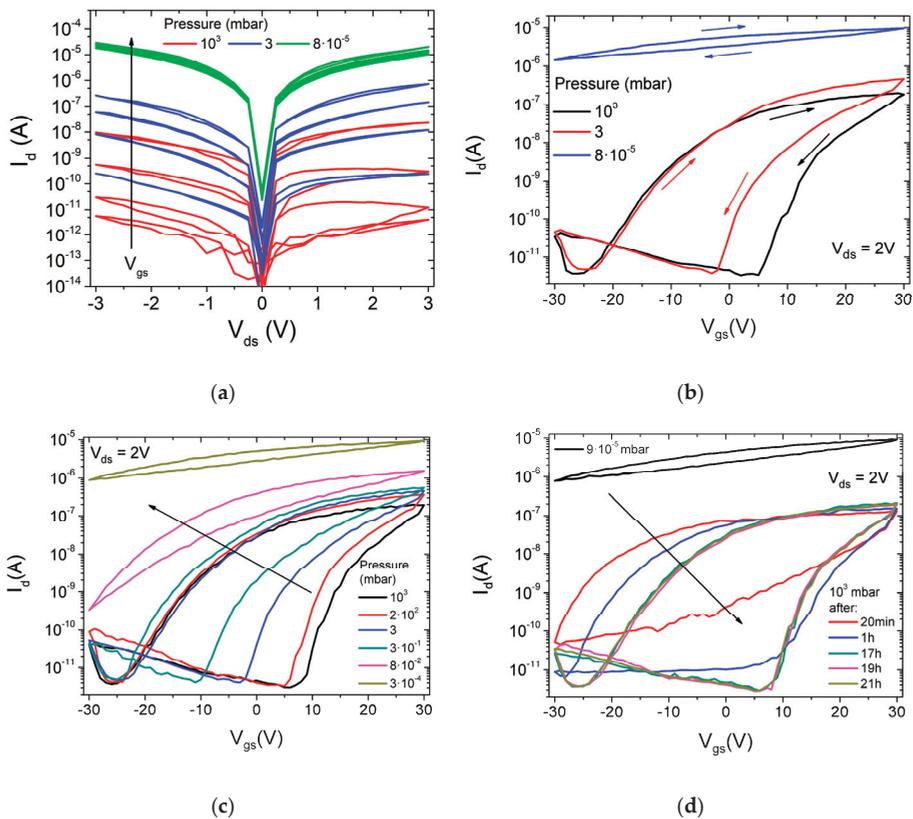


Figure 3. (a) Output curves at different gate voltages ($V_{gs} = 0, 10, 20, 30$ V) for three different air pressures (atmospheric, 3 mbar, 8×10^{-5} mbar). (b) Transfer curves for three different air pressures (atmospheric, 3 mbar, 8×10^{-5} mbar). The arrows show the direction of voltage gate sweeping starting from 30 V. Transfer characteristics (c) for lowering pressure, and (d) at different times after reaching the room pressure.

The same trend with increased current and reduced hysteresis at low pressure is displayed also by the transfer characteristics in Figure 3b. The low pressure, in particular, causes a dramatic change in the transfer characteristics with the transistor that does not turn off over the applied V_{gs} range. The lowering pressure causes a left shift in the transfer

characteristics, corresponding to a reduction in the threshold voltage V_{th} , pointing to an increased n-type doping density. Such behavior can be explained as desorption of adsorbates from the ReSe₂ surface. Adsorbed oxygen and water molecules, being electronegative, subtract electrons to the channel, thus, decreasing the conductivity (otherwise stated, oxygen and water counter-dope the n-type channel with holes). Their desorption has the two-fold beneficial effect of increasing the n-type doping and the mobility (see following), resulting in increased conductivity.

Figure 3c,d, which display the transfer characteristics for lowering and raising pressures, respectively, demonstrate that the transformation of the transfer curves is gradual and reversible. While the plot in Figure 3c shows the dynamic evolution of the transfer curves during the pressure change, the plot in Figure 3d monitors the time evolution of the transfer curves after a sudden change from 8×10^{-5} mbar to room pressure, showing that the recovery of the pristine state is a slow process, requiring a few hours. The reversible change of current with pressure demonstrates that the device can be used as an air pressure gauge.

Figure 4a,b detail the behavior of the mobility μ_{FE} and of the current in the on state (I_{on}) as a function of pressure. The mobility was evaluated using both the forward (V_{gs} sweep from -30 V to 30 V) and reverse (V_{gs} sweep from 30 V to -30 V) branches of transfer characteristics. Both forward μ_{FE} and I_{on} decrease for increasing pressure, following a power law, as demonstrated by the linear log–log plots in the respective insets. Conversely, the threshold voltage V_{th} increases up to 10^{-1} mbar, above which it reaches a plateau (Figure 4c), demonstrating that the desorption of the adsorbates becomes effective at a pressure below 10^{-1} mbar. Finally, Figure 4d shows that the hysteresis width (here defined as the difference between the V_{gs} corresponding to the current $I_d = 1$ nA in the reverse and forward sweep) is also increased by the rising pressure. The contribution of adsorbates to hysteresis in 2D-material-based transistors has been widely studied and demonstrated [34,40,41]. The easier the charge transfer between the channel and the adsorbates, the wider the hysteresis [38].

3.3. Photoresponse

As ReSe₂ nanosheets have been widely used in efficient photodetectors [7,13,42], we checked the photoresponse of the ReSe₂ FET by exposing it to the light of an array of white LEDs at a pressure of 8×10^{-5} mbar.

Figure 5a shows that the current I_d decreases when the device is illuminated, a phenomenon referred to as negative photoconductivity. The decrease in the current under light is enhanced at $V_{gs} = 30$ V. Illumination normally generates additional carriers in a semiconductor material, which increase its conductivity. Conversely, negative photoconductivity has been reported in a few 1D and 2D materials, and explained as a photogating effect due to trap centers, light-induced desorption of surface gas molecules or surface plasmons [43–47]. The origin and role of the negative photoconductivity in low-dimensional materials is still poorly understood. Moreover, negative photoconductivity has not been observed before in ReSe₂ and requires deep investigation that will be the subject of a forthcoming study. Here, we note that the photocurrent ($I_{ph} = I_{light} - I_{dark}$) increases with the drain bias and has the absolute value tunable by the gate voltage, as shown in Figure 5b. The increase in the photocurrent with V_{ds} is easily understood because a higher horizontal field favors charge collection to the drain. The increasing $|I_{ph}|$ with the higher gate bias instead suggests a mechanism for the negative photoconductivity, as gate-induced photo-excited charges separation and trapping. The photogenerated electron-hole pairs are separated by the vertical gate field, which attracts electrons at the ReSe₂/SiO₂ interface, where they become trapped. The excess holes in the channels combine with electrons of the n-type ReSe₂, causing a counter-doping effect, i.e., a reduction in the channel conductivity.

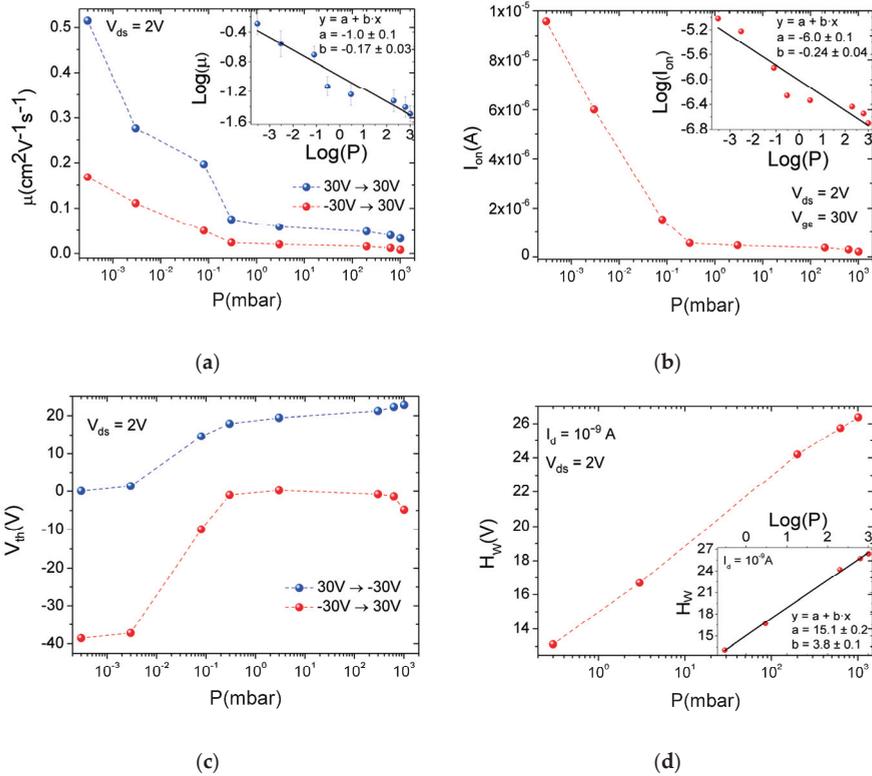


Figure 4. (a) Forward and reverse mobility as function of pressure. Linear fit of the data on log–log scale in the inset, (b) current in the on state as function of pressure. Linear fit of the data on log–log scale in inset, (c) forward and reverse threshold voltage as function of pressure, and (d) hysteresis width at $I_d = 1$ nA versus air pressure. Linear fit of data on semi-log scale in the inset.

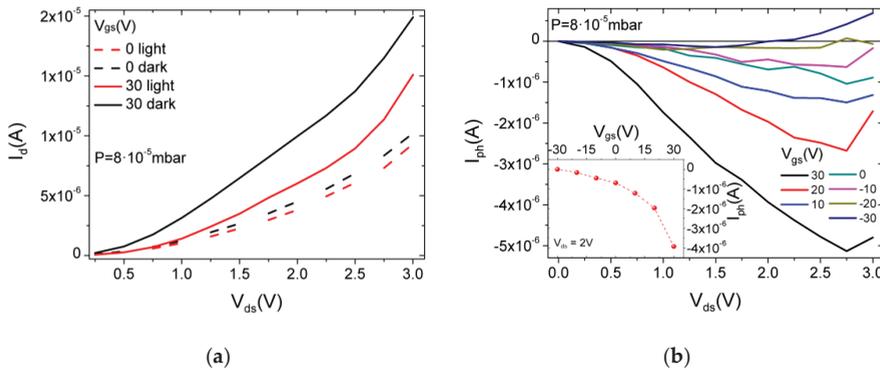


Figure 5. (a) $I_{ds} - V_{ds}$ curves in dark and light at $V_{gs} = 0$ and $+30$ V (dashed and solid lines); (b) $I_{ph} - V_{ds}$ curves at different V_{gs} . I_{ph} vs. V_{gs} at $V_{ds} = 2$ V in the inset.

4. Conclusions

We fabricated a back-gate field-effect transistor with ReSe₂ nanosheets and Cr/Au contacts and studied its electric transport. We showed that the transistor has a dominant n-type character due to the alignment of the Cr Fermi level with the ReSe₂ conduction band minimum. We investigated the effect of low pressure on the material conductivity and found that the device is strongly affected by air pressure. The exposure to air suppresses the channel conductivity as an effect of electron capture by oxygen and water molecules adsorbed on the material surface. The desorption of adsorbates in high vacuum increases the channel conductivity. We pointed out that the reversible pressure behavior allows the device to be used as an air pressure gauge. Furthermore, we showed that the n-type channel and the gate-driven separation and trapping of photogenerated electrons can lower the channel conductivity under illumination, the origin of the observed negative photoconductivity.

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Article

Role of Junctionless Mode in Improving the Photosensitivity of Sub-10 nm Carbon Nanotube/Nanoribbon Field-Effect Phototransistors: Quantum Simulation, Performance Assessment, and Comparison

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Abstract: In this article, ultrascaled junctionless (JL) field-effect phototransistors based on carbon nanotube/nanoribbons with sub-10 nm photogate lengths were computationally assessed using a rigorous quantum simulation. This latter self-consistently solves the Poisson equation with the mode space (MS) non-equilibrium Green's function (NEGF) formalism in the ballistic limit. The adopted photosensing principle is based on the light-induced photovoltage, which alters the electrostatics of the carbon-based junctionless nano-phototransistors. The investigations included the photovoltage behavior, the I-V characteristics, the potential profile, the energy-position-resolved electron density, and the photosensitivity. In addition, the subthreshold swing–photosensitivity dependence as a function of change in carbon nanotube (graphene nanoribbon) diameter (width) was thoroughly analyzed while considering the electronic properties and the quantum physics in carbon nanotube/nanoribbon-based channels. As a result, the junctionless paradigm substantially boosted the photosensitivity and improved the scaling capability of both carbon phototransistors. Moreover, from the point of view of comparison, it was found that the junctionless graphene nanoribbon field-effect phototransistors exhibited higher photosensitivity and better scaling capability than the junctionless carbon nanotube field-effect phototransistors. The obtained results are promising for modern nano-optoelectronic devices, which are in dire need of high-performance ultra-miniature phototransistors.

Keywords: junctionless; zigzag carbon nanotube; armchair-edge graphene nanoribbon; quantum simulation; sub-10 nm; phototransistors; photosensitivity; subthreshold swing

1. Introduction

Optoelectronic devices based on carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), namely, GNR/CNT-based cells, carbon-based phototransistors, and carbon-based photodetectors, have attracted significant interest in recent years [1–5]. Indeed, CNT/GNR-based phototransistors have gained keen focus owing to their promising features such

as the unique light–CNT/GNR interaction, high photoresponsivity, fast response, high detectivity, high photosensitivity, extensive detection range, and especially, the low noise in comparison to the conventional photodiodes [6–10]. Most of these promising features are attributed to the unique characteristics that the CNTs and GNRs exhibit in terms of the physical, electrical, optical properties and are synergistically correlate with their atomistic structures [11,12]. Therefore, the applications of the CNT/GNR-based phototransistors are highly effective in imaging, optical communication, and sophisticated (bio)sensing applications (e.g., the photoplethysmography) [13], which makes them suitable for futuristic nano-optoelectronics.

The photogating paradigm is one of the most efficient and straightforward principles in phototransistors that allows the conversion of the light information into an electrical signal (change in drain current) through light-induced electrostatic and transport modulations [6,14–16]. In fact, the concept of the light-induced gate photovoltage [17] has given the ability to mostly confine the light's electrical effect at the sensitive component (i.e., the photogate), and thus the field-effect devices act as transducers while greatly simplifying the photosensing mechanism, which is somewhat complicated when the light affects all phototransistor components including the sensing and transducing parts [18,19]. Recently, the light-induced photovoltage approach has made it possible to simply combine cutting-edge field-effect transistors, generally based on emerging 2D materials, with particular photosensing gates while forming advanced high-performance phototransistors [20–22]. In this context, some improvement approaches have been proposed to boost the modern carbon-based phototransistors such as, the use of an ultra-sensitive photogate producing improved photovoltage under specific illumination [23,24], exploiting the high-sensitivity of the GNR channel to the light-induced electrostatic modulation [22], and the identification of a photosensing regime, in which the phototransistors can provide better photosensing performance [10]. However, to the best of our knowledge, the role of the junctionless (JL) paradigm in improving the sub-10 nm CNT/GNR phototransistors and the performance comparison between ultrascaled CNT-based phototransistors and ultrascaled GNR-based phototransistors in junctionless mode and inversion mode (IM) are still questionable, which deserves experimental and computational investigation. More importantly, it is obvious that, with the continuous miniaturization of modern electronics and the progress experienced in large-scale integration, optoelectronics needs high-performance, easy-to-make, and miniature (sub-10-nm) phototransistors [10].

Further, doping is an essential process for ensuring the appropriate functioning of nanotransistors. Implant and/or diffusion processes are commonly used to create chemical doping in semiconductors, wherein the process and material parameters such as implantation dose, energy, diffusion time, temperature and solid solubility limit play a crucial role in determining the doping profile of concentration and junction depth. However, for CNT, graphene, and the other 2D-material-based FETs, the chemical route of doping is quite cumbersome as these nanoscale devices demand the formation of very high doping gradient-based junctions [25]. Therefore, electrostatic doping, which potentially replaces the conventional donor/acceptor dopant-based chemical doping with image charge, i.e., free-electron/hole, has been adopted for nanoscale devices [26–28]. The difference in the photosensitive gate and CNT/GNR work function, applied voltage, energy bandgap, trap engineering, and their interactions result in an electrostatic connection that governs the carrier density for the formation of the p-channel in the proposed phototransistor. Electrostatic doping allows the formation of a virtual junction near the source and drain by emulating a p-channel beneath the polarity gate, where it has merit in controlling the concentration by applying a specific voltage to the polarity gate electrode. This technique also results in formation of ultra-sharp junctions with a controlled doping profile with the feature of lower defect density. Therefore, the foundation of utilizing the junctionless technology in designing the proposed phototransistor mitigates the limitations such as high thermal budget, random dopant fluctuations, and costly millisecond annealing techniques, also known as rapid thermal annealing [29].

In this regard, for the first time, this study assesses the role of junctionless mode in improving the photosensing performance of GNR/CNT-based sub-10 nm phototransistors while targeting the facility of fabrication and improving the electrical and photosensing performance. In addition, this computational investigation fairly compares the IM/JL CNT phototransistors performance against the IM/JL GNR phototransistors' performance, while deeply analyzing the relevant quantum transport including the impact of bandgap, effective mass, and tunneling components on the photosensing performance. The numerical investigation proposed in this paper is based on a quantum simulation, which self-consistently solves the Poisson solver and the mode-space non-equilibrium Green's function (NEGF) formalism in the ballistic limit, where the Hamiltonian of GNR and CNT, which have been presented in previous works, have been normally employed in the NEGF computation [30–33]. The double-gate (DG) configuration has been adopted for the JL/IM GNR-based phototransistors, while the coaxial-gate (CG) geometry has been considered for the JL/IM CNT-based phototransistors. The presented study included the transfer characteristics, the photosensitivity, the dependence subthreshold swing-photosensitivity, quantum transport (energy bandgap, effective mass, direct and band-to-band tunneling currents), the photo-electrostatics, and the impact of change in CNT/GNR energy bandgap (through diameter/width variation) on the subthreshold domain, which was adopted as photosensing regime.

The rest of this paper is organized as follows: Section 2 presents the nano-phototransistors structures. Section 3 summarizes the adopted NEGF-based quantum simulation approach. Section 4 shows and analyzes the results. Section 5 is a conclusion outlining the main findings of the investigation presented in this paper.

2. Device Structure

Figure 1a shows a sketch of the two-dimensional armchair-edge GNR (AGNR) with its detailed atomic structure. It is a well-known fact that the bandgap of AGNR depends on its width [11,34]. Therefore, in this investigation, we considered the semiconducting families (i.e., $n = 3p$ and $n = 3p + 1$). Simultaneously for a fair comparison, the ZCNT bandgap was also accounted for. Figure 1b shows a schematic of the ZCNT. Similar to AGNR, the bandgap of the ZCNT depends on its diameter, thus we considered the appropriate diameters in this comparative study [35]. It can be clearly noted from Figure 1a,b that the ZCNT can be formed by rolling the AGNR. This important aspect tremendously simplifies the quantum simulation in terms of NEGF computations in mode-space (MS) representation [35–37]. However, from the point of view of the electrostatics, the coaxial-gate configuration and double-gate structure were treated differently using the finite difference method (FDM) and finite element method (FEM). Figure 1c shows the 3D perspective of the ultrascaled double-gate junctionless graphene nanoribbon field-effect phototransistor. An AGNR is considered as channel material, which is sandwiched between two hafnium oxide layers. The germanium-based photogates are placed at the medium of the nanodevice over and under the oxide materials. Figure 1d shows the three-dimensional (3D) structure of the ultrascaled coaxially photogated junctionless carbon nanotube field-effect phototransistor. A zigzag-type carbon nanotube is considered as channel material, which is coaxially sandwiched in a hafnium oxide cylinder acting as an insulator. Note that the use of high- k HfO_2 oxide in the two carbon-based phototransistors aims to provide a good electrostatics control over the carrier transport [35–37]. The germanium-based photogate is placed at the nanodevice medium with a gate-all-around (GAA) configuration. The source and drain electrode are clearly shown in the same figure while assuming an ohmic contact. Figure 1e shows the lengthwise cut view of both carbon-based nano-phototransistors. As shown, the cross-sectional view is similar with the same components, materials (excepting the channel material), and parameters. We emphasize that the interior of the zigzag carbon nanotube is considered an air environment [35]. Figure 1f shows the considered junctionless n-type doping in both nano-phototransistors, devoid of metallurgical junctions that complicate the nanofabrication of such ultrascaled transistors [29,38]. It is worth noting

that the main benefits of junctionless FETs are the simplification of fabrication on one hand and the improvement in subthreshold behavior on the other hand [38–40]. From the fabrication point of view, the production of an array configuration of such nanodevices is expected to be profitable since the elementary devices can be manufactured identically [41], because no junctions and no doping concentration gradients are needed [29,38]. Table 1 shows the physical, dimensional, and electrical parameters of the nanoscale carbon-based phototransistors under investigation. The doping molar fraction in both FETs is taken to be comparable [30–32]. It is important to note here that a low source-to-drain bias is considered ($V_{DS} = 0.3$ V), which is beneficial for low-power photosensing applications. It is worth noting that the diameter of the ZCNT and the width of the AGNR, which are tunable parameters to reach a suitable bandgap, were intentionally chosen to provide a comparable energy bandgap for fair comparison.

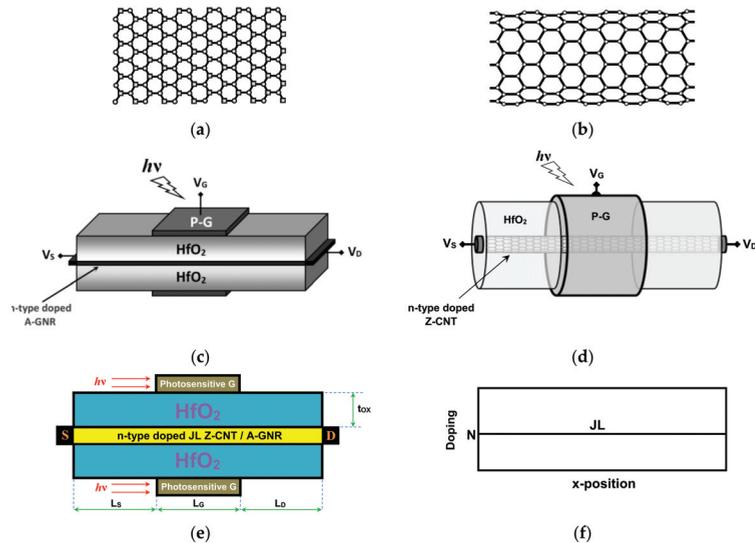


Figure 1. Sketch of (a) armchair-edge graphene nanoribbon and (b) zigzag carbon nanotube. (c) The 3D structure of a double-photogate junctionless graphene nanoribbon field-effect phototransistor. (d) The 3D structure of a coaxial-photogate junctionless carbon nanotube field-effect phototransistor. (e) Lengthwise cut view of the ultrascaled JL carbon nanotube/nanoribbon field-effect phototransistors under study. (f) Uniform n-type doping profile of the junctionless phototransistors under investigation.

Table 1. The physical, dimensional, and electrical parameters of DGJL GNRFET and GAAJL CNTFET.

Parameter	Symbol	DG JL GNRFET	GAA JL CNTFET	Unit
Dimmer number	n	13	13	-
Bandgap	E_G	~0.86	~0.81	eV
Width/diameter	W_{GNR}/d_{CNT}	~1.47	~1	nm
Sensitive gate length	L_G	8	8	nm
S/D length	$L_{S(D)}$	10	10	nm
S/C/D doping	$N_{S/C/D}$	0.56	1.5	nm^{-1}
Oxide thickness	t_{OX}	1.5	1.5	nm
Oxide dielectric constant	ϵ_{OX}	16	16	-
Temperature	T	300	300	K
Light wavelength	λ	1550	1550	nm
Drain-to-source voltage	V_{DS}	0.3	0.3	V

3. Quantum Simulation Approach

The computational treatment of the armchair-edge graphene nanoribbon and the zigzag carbon nanotube using the mode-space (MS) non-equilibrium Green's function (NEGF) is comparable due to the crystalline similarity between the AGNR and the ZCNT from the mode-space representation point of view [30–33,42,43]. It can be deduced from this comparison that the main difference resides in the Hamiltonian [30–33]. Note that the edge bond relaxation is normally considered in the AGNR's case [30]. As shown in the flowchart of the used quantum simulation method, a potential vector is employed as an initial guess to start the self-consistent procedure between the Poisson equation and the NEGF solver. This latter is initially based on the computation of the retarded Green's function, which is well known and is defined as follows [44,45]:

$$G(E) = [(E + i\eta^+)I - H_{PZ} - \Sigma_S - \Sigma_D]^{-1} \quad (1)$$

where E , η^+ , H_{PZ} , I , and $\Sigma_{S(D)}$ are the energy, infinitesimal number, ZCNT/AGNR Hamiltonian matrix based on the atomistic nearest neighbor p_Z -orbital tight-binding (TB) approximation [30–33], identity matrix, and the source (drain) self-energy, respectively. It is worth indicating that the mode-space fashion was adopted in the simulation of both nano-phototransistors in order to save the computational cost [36], which is ordinarily pronounced when using the real-space approach [46]. It is important to note that only the first subband was considered in both cases, which is sufficient from an accuracy point of view [30–32]. The energy level broadening due to the source (drain) contact, $\Gamma_{S(D)}$, and the source (drain) local density of states, $D_{S(D)}$, can now be obtained using the following equations [30–32]:

$$\Gamma_{S(D)} = i(\Sigma_{S(D)} - \Sigma_{S(D)}^\dagger) \quad (2)$$

and

$$D_{S(D)} = G\Gamma_{S(D)}G^\dagger \quad (3)$$

The charge density in AGNR and ZCNT channels can be normally computed using the above NEGF quantities based on the following expression [30–32]:

$$Q_{GNR/CNT}(x) = (-q) \int_{-\infty}^{+\infty} dE \cdot \text{sgn}[E - E_N(x)] \times \{D_S(E, x) f(\text{sgn}[E - E_N(x)](E - E_{FS})) + D_D(E, x) f(\text{sgn}[E - E_N(x)](E - E_{FD}))\} \quad (4)$$

where q , sgn , E_N , f , and $E_{FS(FD)}$ are the electron charge, sign function, charge neutrality level, Fermi function, and source (drain) Fermi level, respectively. As shown in Figure 2, the flowchart of the quantum simulation has a self-consistent procedure, which means that the NEGF solver needs the electrostatic information and the Poisson solver needs a channel charge information. Therefore, the electrostatics should be estimated by solving the Poisson's equation using the finite difference method (FDM) considering the nano-phototransistors' geometry [30–32,47]. It is worth noting that the Neumann boundary conditions were considered for the external interfaces including the source and drain electrodes excepting the applied voltage nodes, which were treated considering the Dirichlet boundary condition, where the photosensing paradigm is embedded by adding to the applied gate voltage, V_{GS} , the so-called light-induced photovoltage, V_{PH} . Hence, the resulting effective gate voltage, V_{GS-EFF} , can be expressed as follows [10,17]:

$$V_{GS-EFF} = V_{GS} + V_{PH} \quad (5)$$

Considering a Ge-based photogate, the photovoltage V_{PH} can be empirically expressed as a function of the incident optical power (P_{INC}) [17]

$$V_{PH} = (nkT/q) \times \ln [1 + (\eta q P_{INC}) / (hv I_S)] \quad (6)$$

where k , n , T , hv , I_S , and η are Boltzmann constant, empirical constant (taken to be 0.4), temperature, photon energy, diode leakage current, and quantum efficiency, respectively [10–17].

It is worth noting that the junctionless mode (inversion mode) is computationally treated in the second term of the Poisson equation by considering the same doping concentration (the intrinsic portion) at the channel underneath the gate within the concerned nodes in the FDM.

After obtaining the computational convergence, the current can be calculated by the following integral [30–32]:

$$I = \frac{xq}{\hbar} \int_{-\infty}^{+\infty} dE T(E) [f(E - E_{FS}) - f(E - E_{FD})] \tag{7}$$

where \hbar is the Planck’s constant, x is taken to be 4 for CNT and 2 for GNR, and $T(E)$ is the transmission coefficient given by

$$T(E) = Tr [\Gamma_S G \Gamma_D G^\dagger] \tag{8}$$

where Tr is the trace operator. Now, the photosensitivity is within reach and can be computed as

$$Ph = \frac{I_{ILLUM} - I_{DARK}}{I_{DARK}} \tag{9}$$

where I_{DARK} denotes the I_{DS} in dark condition and I_{ILLUM} is the drain current under illumination. For more details about the computational methodology, we refer to some relevant works [46–48].

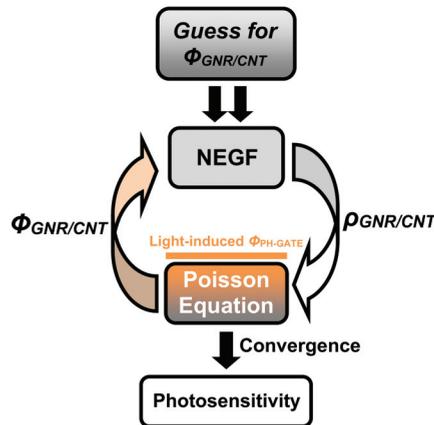


Figure 2. Flowchart of the self-consistent computational approach that considers the Poisson equation solver and the mode-space NEGF solver.

4. Results and Discussion

As known, NEGF-based quantum simulation is a powerful conceptual method and a practical analysis approach to deal with nanoelectronic devices including modern nanotransistors, where the quantum effects, specific electrostatics, and atomistic features play a pivotal role. In fact, the adopted quantum simulation approach contains several computational blocks including the FDM-based Poisson solver, the NEGF-based Schrodinger solver, the non-linear dummy function for convergence efficiency, and an analytical relation describing the light-induced photovoltage. For this reason, the source code of the quantum simulators should be checked while reasonably comparing their outputs with some works in the literature [17,30,32]. For precision’s sake, we compared the simulated I_{DS} - V_{DS} output characteristics of the baseline GNR-FET and CNT-FET with those reported

in relevant simulation works considering the same conditions (i.e., ballistic transport), gating configurations, and physical and geometrical parameters and the same simulation approach [30,32]. As shown in Figure 3, an excellent agreement was obtained for both nanotransistors while confirming the soundness and accuracy of the simulator source code. The recorded excellent matching is normally attributed to the use of same simulation parameters, fine spacing mesh in the FDM-based Poisson solver, and efficient non-linear dummy function to speed up and ensure self-consistency.

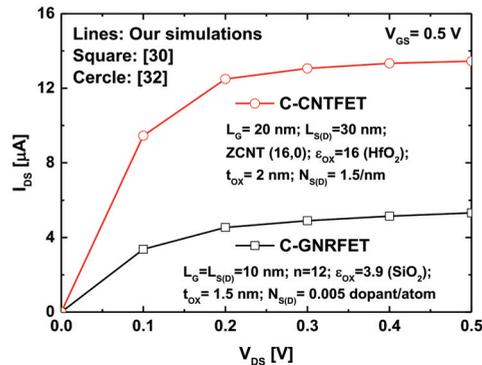


Figure 3. The I_{DS} - V_{DS} output characteristics of the baseline double-gate GNRFET and coaxially gated CNTFET. Lines: results issued from the simulator, symbols: results obtained in [30,32].

Figure 4a shows the experimentally measured photovoltages [17] as a function of the theoretically calculated ones using the above-mentioned empirical relation (Equation (6)) [17]. As shown, a good agreement was noticed for a wide range of incident optical power. Figure 4b shows the Ge photovoltage as a function of the incident optical power considering a monochromatic light wavelength of 1550 nm. It is worth indicating that the curve issued from the empirical relation (Equation (6)) showed excellent agreement with experimental data [17]. Note that the light-induced photovoltage can behave better for a given wavelength and incident optical power by improving the crystal quality and/or applying surface treatments [17]. Other engineered materials [23,24] can also be employed as photosensing gates with some consideration to the band bending. Inspecting the same figure, we can see that the considered range of incident optical power can generate an exploitable amount of photovoltage especially if the nano-phototransistor is operated in the subthreshold regime, where the drain current is more sensitive to the variation of the effective gate voltage [42]. In the literature, it is well known that the FET-based sensors operating with the sensing principles of the measurand-induced modulation in gate voltage are preferably operated in the subthreshold domain targeting optimal sensitivities [42]. In this context, we will show how the junctionless paradigm can not only facilitate the fabrication process by avoiding the integration of sharp junctions but also boost the photo-sensitivity making the proposed carbon-based nano-phototransistors intriguing candidates for the modern nano-optoelectronics, in which fabrication reliability and high performance are prerequisites.

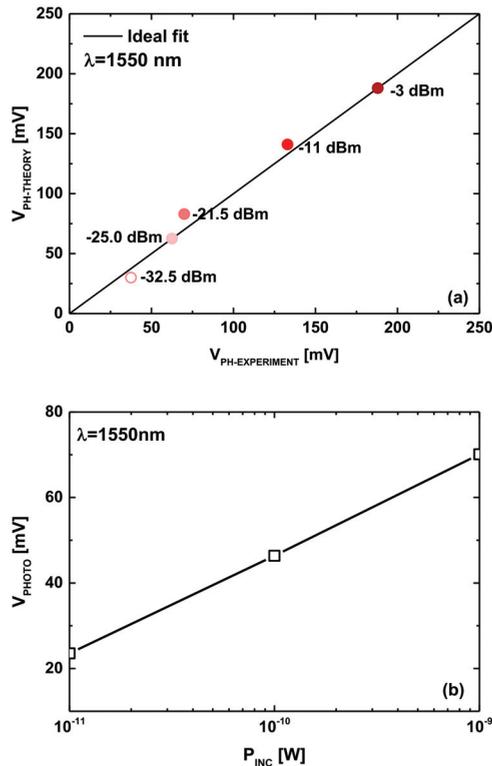


Figure 4. (a) The measured photovoltage [17] versus the modeled photovoltage. (b) The light-induced photovoltage as a function of incident optical power in Ge-based photosensing gate.

In order to clearly show the impact of the infrared light illumination on the quantum transport of the sub-10 nm carbon-based junctionless nano-phototransistors under investigation, we obtained from the NEGF quantities, the electron density spectrum (or equivalently, the energy-position-resolved electron distribution) [31,32] considering a gate bias near the threshold voltage condition. Under the dark condition, we can see in Figure 5a,c that there was no electron flow over the potential barrier, which means that both nanophototransistors were in the optical off-state regime. However, the direct source-to-drain tunneling mechanism (shown in the same figure in the form of some tunneling states through the potential barrier) exists normally due to the considered ultrascaled photogate lengths (sub-10 nm) [35,48,49]. It is worth noting that the junctionless paradigm is found to be very efficient in mitigating the leakage current in both carbon nanotube- and nanoribbon-based nanoFETs, which is very beneficial for low-power optoelectronic systems [39,40]. Under illumination with a monochromatic light with 1550 nm wavelength and 1 nW as incident optical power, we observed a flow of electron from source to drain over the potential barrier, which is attributed to the light-induced photovoltage that lowers the potential barrier while allowing a thermionic emission, which was clearly visible by light spectrum over the barrier from left to right. This behavior explicitly indicates the record of photosensitivity to the considered monochromatic light.

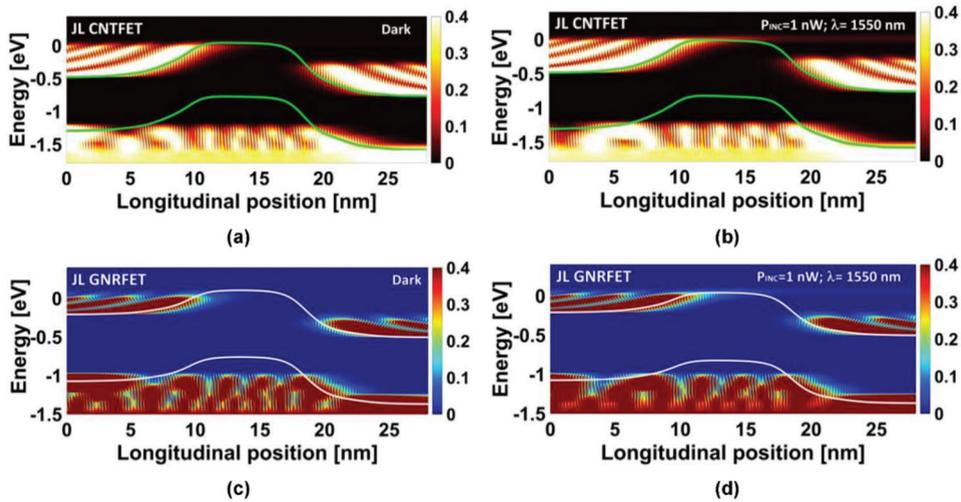


Figure 5. Color-scaled plot for the energy-position-resolved electron distribution along the ZCNT for the JL CNTFET (top figures) and JL GNRFET (bottom figures). The plots (a,c) are drawn under dark condition, while the plots (b,d) are drawn under illumination condition ($P_{INC} = 1 \text{ nW}$, $\lambda = 1550 \text{ nm}$).

Figure 6 shows the potential distribution of the DG GNRFET-based phototransistor with 8 nm photogate length in dark and illumination conditions, where $\lambda = 1550 \text{ nm}$ and $P_{INC} = 1 \text{ nW}$ were considered. We can see the effect of the photogating (i.e., underneath the Ge photogate) in Figure 6b, where a reduction at the level of potential profile (i.e., 10–18 nm) was recorded in comparison to the dark case in Figure 6a, which is expected according to the gate photovoltage-based photosensing principle. By comparing the two figures, we also observed a shrinking in terms of the potential barrier width in the illumination case. However, no substantial electrostatic modulations were recorded far from the photo-gating region, where the nano-phototransistor was ungated.

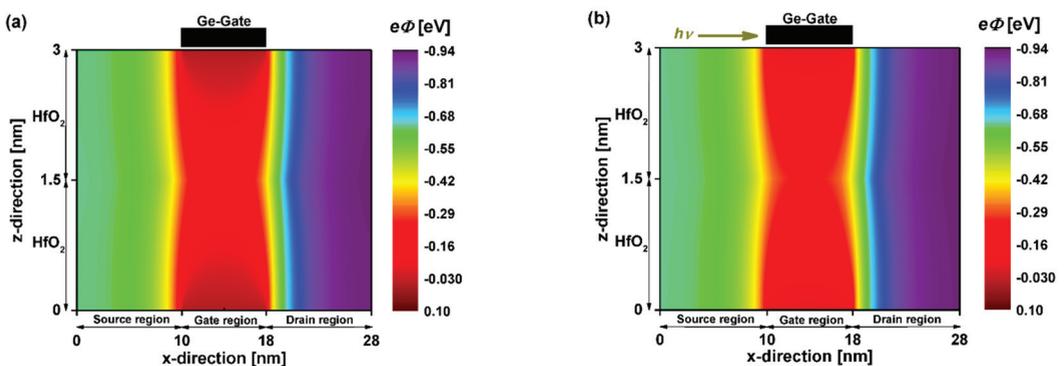


Figure 6. Two-dimensional potential distribution of the sub-10 nm double-gate junctionless carbon nanoribbon field-effect phototransistor before (a) and after (b) illumination with: $V_{DS} = 0.3 \text{ V}$ and $V_{GS} = 0 \text{ V}$. The infrared light-induced photovoltage is $V_{PH} = 0.07 \text{ V}$.

Figure 7 shows the 2D potential distribution of the coaxially photogated CNT field-effect phototransistors extracted after the self-consistency at the longitudinal cross-section (a,b) and the middle cross-section (c,d) of the nanodevice before and after the IR illumi-

nation. As recorded in the case of the JL GNR-based phototransistor, the JL CNT-based nano-phototransistor exhibited the same behavior, where the IR illumination-induced reduction in electrostatic gating was clearly pronounced by comparing the dark and light scenarios shown in Figure 7a,c and Figure 7b,d, respectively.

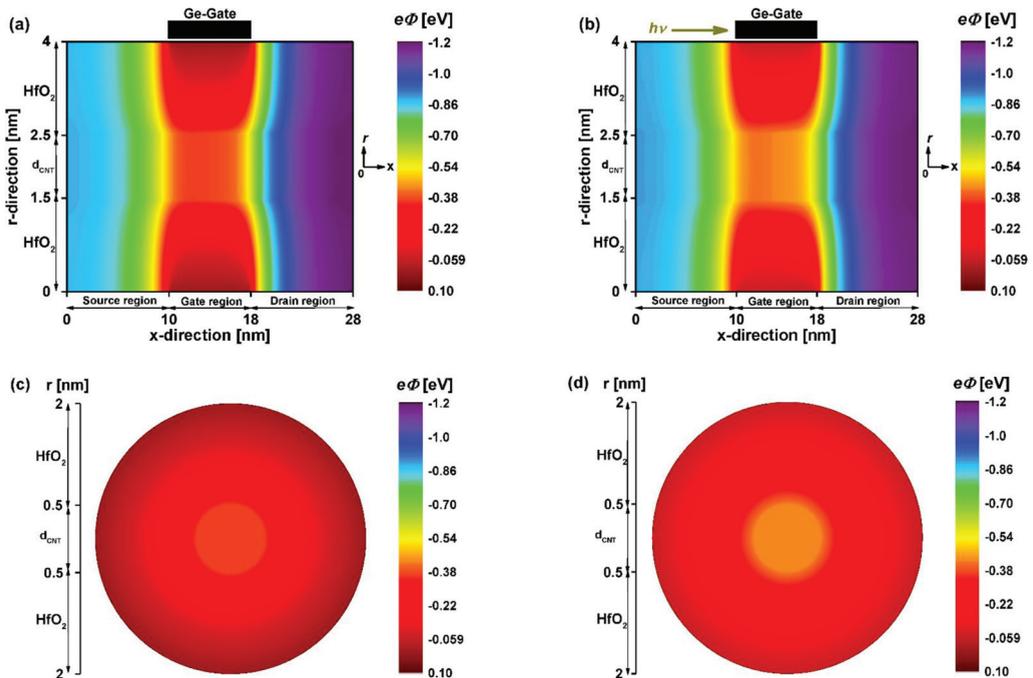


Figure 7. 2D potential distribution of the 8 nm coaxial-gate junctionless carbon nanotube field-effect phototransistor before (a,c) after (b,d) illumination at $V_{DS} = 0.3$ V. The top figures are drawn from the nodes at the lengthwise cut view, while the bottom figures are extracted from the nodes at the middle cross-section of the nano-phototransistor. $V_{PH} = 0.07$ V is considered as an infrared light-induced photovoltage.

Figure 8 shows the maximum photosensitivities of the nanoscale carbon-based phototransistors under investigation, which were drawn from the subthreshold photosensing regime due to the high sensitivity that it can provide toward the measurand-induced effective V_{GS} modulation [42]. As shown, the junctionless nanoscale carbon-based phototransistors exhibited higher photosensitivities than those provided by inversion-mode nanoscale phototransistors. In addition, on comparing the IM GNR/CNT-based nanoscale phototransistors, the IM-GNRFET exhibited higher photosensitivity than that provided by IM-CNTFET; equivalently, the IM-GNRFET exhibited a steeper optical subthreshold swing. A similar observation was recorded for the junctionless nano-phototransistors, where the JL-GNRFET provides higher photosensitivity than its JL-CNTFET counterpart.

In order to understand the superiority of junctionless nanoscale phototransistors over the inversion-mode nanoscale phototransistors in terms of photosensitivity, we plotted in Figure 9 the transfer characteristics and the potential profile of the ultrascaled carbon-based phototransistors under investigation. Inspecting Figure 9a,b showing the transfer characteristics, we can clearly observe that the junctionless paradigm improved the I_{DS} - V_{GS} propriety of both carbon-based nanoscale photo-FETs, where a decrease in off-current is clearly visible leading to an improvement in terms of subthreshold swing and current while

explaining the superiority of JL photo-FETs over IM photo-FETs in terms of photosensitivity, as shown in Figure 8. It is worth noting that the steeper SS is, the higher photosensitivity is, since the photosensing principle is based on the light-induced gate photovoltage and because the subthreshold swing can be viewed as the sensitivity of drain current to the variation in effective gate voltage [49–52]. Figure 9c,d show how the junctionless mode improves the subthreshold characteristics by lowering the leakage current and decreasing the swing factor. As shown, the consideration of the junctionless paradigm or, equivalently, the uniform n-type doping profile, dilated the potential barrier while mitigating the direct source-to-drain tunneling (DSDT), which is more significant in sub-10 carbon nanotube/ribbons-based FETs [39,40]. This junctionless-mode-induced immunity against the DSDT leakage explains the recorded decrease in off-current and subthreshold swing, which were the physical cause of the recorded enhancement in photosensitivity.

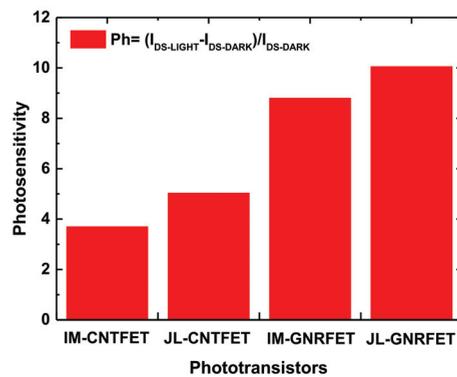


Figure 8. Photosensitivity of IM/JL CNTFET- and IM/JL GNRFET-based nano-phototransistors.

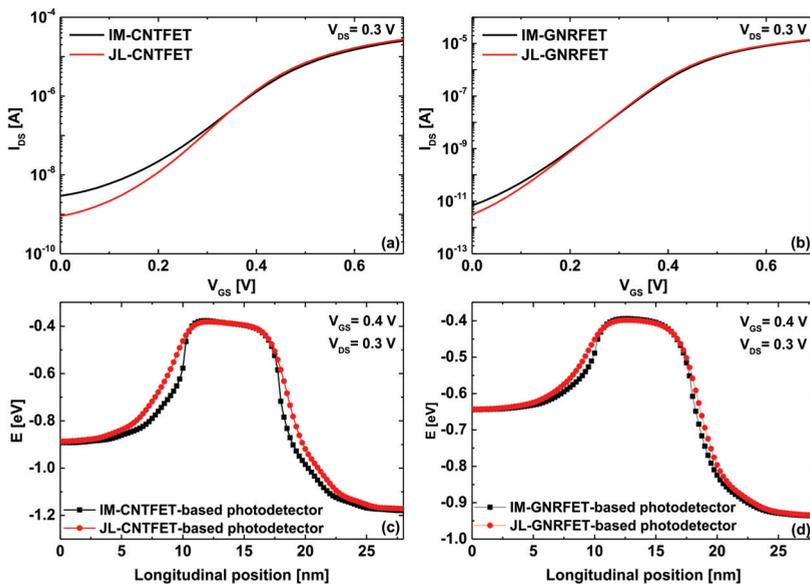


Figure 9. Transfer characteristics of (a) IM/JL-CNTFET and (b) IM/JL-GNRFET. The potential profile of (c) IM/JL-CNTFET and (d) IM/JL-GNRFET at $V_{GS} = 0.4$ V and $V_{DS} = 0.3$ V.

In the literature, the impact of change in the width (diameter) of the carbon nanoribbon (nanotube) on the GNR(CNT)FET's subthreshold performance has been found significant because of the bandgap/effective mass-width (diameter) dependence [32,42]. For this reason, we plotted in Figure 10 the subthreshold swing and photosensitivity of the nanoscale carbon phototransistors as a function of energy bandgap and diameter/width variation. As described above, the steep nano-FETs (i.e., having low subthreshold swing) are logically expected to have high photosensitivity basing on the principle of the light-induced gate photovoltage. For this reason, we can see in the three plots of Figure 10 that the photosensitivity increased with the subthreshold swing's decrease. Inspecting the figures, one can also see that the diameter/width-decrease-induced energy bandgap energy increase improved the subthreshold swing and photosensitivity of JL CNT/GNR phototransistors. This improvement, caused by the diameter/width-decrease-induced energy bandgap increase, can be explained by the mitigation of tunneling currents including the leakage current known as the band-to-band tunneling [52,53]. Inspecting Figure 10a, one can see that the curvature effects, which can be a concern in the reliability of CNTFET performance, can seriously limit the scalability and the efficiency of the improvement technique based on the CNT diameter variation. On the other hand, in the GNRFET's case (for both families), we can see that ultrascaled widths were required to achieve the ideal FET subthreshold swing (i.e., 60 mV/dec) and the ultimate photosensitivity, which is challenging from the fabrication point of view. More importantly, by comparing the GNRFETs with armchair-edge GNRs of $n = 3p$ with those of $n = 3p + 1$ dimer, we can clearly observe that the GNRFETs with $n = 3p + 1$ channels exhibited higher photosensitivity and steeper swing factor than those with $n = 3p$ channels. This is attributed to the larger effective mass of $n = 3p + 1$ GNRs as well as their higher energy bandgap, which allow better switching with improved SS values due to the resulted mitigation in tunneling subthreshold currents. It is worth noting that the third AGNR family of $n = 3p + 2$ was not considered because it contains close-to-metallic GNRs with a very small energy bandgap, which are not suitable for FET applications including the phototransistors as in the graphene field-effect transistor (GFET) [53–55].

The swing factor–photosensitivity dependence described above has beneficial technological implications, such that the engineering of dielectric material and its thickness can be normally adopted to improve the electrostatic gating while converging to the ideal SS [39,40] and the optimal photosensitivity. The doping-engineering-based improvement technique (while keeping the junctionless paradigm) [40] can also be employed to improve the subthreshold characteristics via the dilation in the potential barrier. However, the present uniform doping remains less complicated in the manufacturing process, which is beneficial for mass production and advanced optoelectronics based on array configurations. More importantly, since the JL CNT/GNRFET can provide subthermionic subthreshold swing (very high photosensitivity) when they are operated in band-to-band regime [48,52], the assessment and performance projection of nanoscale BTBT GNR/CNT phototransistor can be an exciting matter for further computational investigations. From another perspective, the steep transistors based on tunneling mechanism [56–58] and negative capacitance paradigm [59–65] can be advanced nano-phototransistors while forming a matter for further investigations.

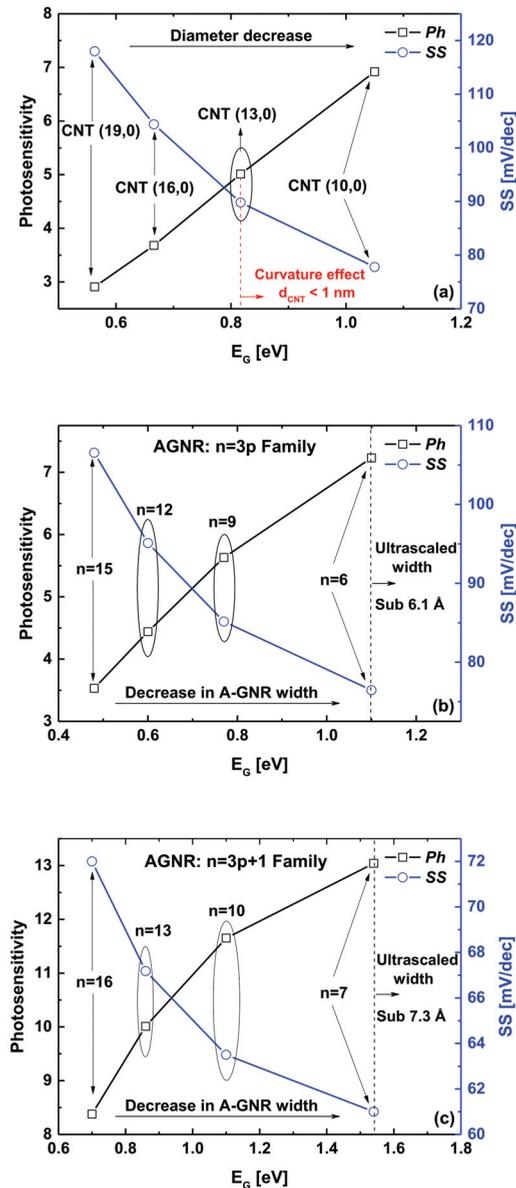


Figure 10. Impact of change in (a) ZCNT diameter and (b,c) AGNR width, on the photosensitivity and SS of the nanoscale phototransistors under investigation. $\lambda = 1550$ nm, $P_{INC} = 1$ nW with $V_{PH} = 0.07$ V.

5. Conclusions

In this paper, carbon-based junctionless phototransistors endowed with sub-10 nm photogate lengths were computationally assessed using the NEGF simulation. The light-induced modulation of electrostatics through the photogate was employed as a photosensing principle. The impact of the light illumination on the transport of carbon-based junctionless phototransistors was thoroughly analyzed via the energy-position-resolved electron density. It was found that the junctionless paradigm is efficient in boosting the

photosensitivity of GNR/CNT-based phototransistors by dilating the potential barrier while mitigating the tunneling currents and improving the subthreshold characteristics; however, the thermionic limit imposed a limitation in terms of photosensitivity in both junctionless phototransistors. From the comparison point of view, the GNR-based junctionless phototransistors exhibited higher photosensitivity than the CNT-based junctionless phototransistors. In addition, we also analyzed the role of change in ZCNT (AGNR) diameter (width), in improving the subthreshold and photosensing performance through the modulation in energy bandgap, where the phototransistors based on AGNR with $n = 3p + 1$ showed intriguing photosensing performance due to the higher effective mass and larger bandgap, which have a direct reflection on the tunneling currents, which are the leading cause of subthreshold swing degradation. Considering the performed comparative analysis on the subthreshold swing–photosensitivity dependence, we believe that the n-n-n JL CNT/GNR field-effect phototransistors operating in the band-to-band regime (i.e., the on-state is controlled by the BTBT current while the off-state is the cause of DSDT current) can open a new way to achieve very high photosensitivity (sub-thermionic subthreshold swing) using an easy-to-make JL-based structure.

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Article

Synergy of Electrostatic and Chemical Doping to Improve the Performance of Junctionless Carbon Nanotube Tunneling Field-Effect Transistors: Ultrascaling, Energy-Efficiency, and High Switching Performance

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Abstract: The low on-current and direct source-to-drain tunneling (DSDT) issues are the main drawbacks in the ultrascaled tunneling field-effect transistors based on carbon nanotube and ribbons. In this article, the performance of nanoscale junctionless carbon nanotube tunneling field-effect transistors (JL CNTTFETs) is greatly improved by using the synergy of electrostatic and chemical doping engineering. The computational investigation is conducted via a quantum simulation approach, which solves self-consistently the Poisson equation and the non-equilibrium Green's function (NEGF) formalism in the ballistic limit. The proposed high-performance JL CNTTFET is endowed with a particular doping approach in the aim of shrinking the band-to-band tunneling (BTBT) window and dilating the direct source-to-drain tunneling window, while keeping the junctionless paradigm. The obtained improvements include the on-current, off-current, ambipolar behavior, leakage current, I_{60} metric, subthreshold swing, current ratio, intrinsic delay, and power-delay product. The scaling capability of the proposed design was also assessed, where greatly improved switching performance and sub-thermionic subthreshold swing were recorded by using JL CNTTFET with 5 nm gate length. Moreover, a ferroelectric-based gating approach was employed for more enhancements, where further improvements in terms of switching performance were recorded. The obtained results and the conducted quantum transport analyses indicate that the proposed improvement approach can be followed to improve similar cutting-edge ultrascaled junctionless tunnel field-effect transistors based on emerging atomically thin nanomaterials.

Keywords: carbon nanotube; junctionless; tunnel field effect transistors; chemical doping; electrostatic doping; NEGF simulation; band-to-band tunneling; switching performance; nanoscale

1. Introduction

Sub-thermionic subthreshold swing provided by nanoscale-tunnel field-effect transistors (TFETs) enables a decrease in power supply voltage, which is a prerequisite in ultralow power applications, such as the internet of things (IoT) [1,2]. In the last decade, the great progress experienced in nanomaterials science have given an additional asset and new

impulses to TFETs technology, which can play a leading role in the extension of Moore's Law that converges to its end [2–5]. In the ultrascaled regime, the accuracy of nanofabrication is crucial for the reliability of elementary nanoelectronic nanodevices, as it can affect the performance of electronic circuits and systems [2–6]. In this context, the junctionless paradigm has shown its efficiency in simplifying the elaboration of ultrascaled FETs on the one hand and in improving their performance on the other hand [6–9]. Combining the benefits of the junctionless paradigm with the amazing features of tunneling transistors has been the subject of promising devices called junctionless-tunnel field-effect transistors (JL TFETs) [9]. In these devices, the channel doping is performed by the electrostatic and chemical doping, while ensuring the operating regime of tunneling FETs with a double benefit in terms of the facility of fabrication and high performance [9,10].

In the literature, the junctionless-carbon-nanotube-tunnel field-effect transistors (JL CNTTFETs) have shown promising subthreshold and switching performance [5,10,11] due to the amazing characteristics of carbon nanotube (CNT) as mature channel material, such as atomic structure, tunable band gap, high electrical conductivity, quasi-ballistic property, high Fermi velocity, and high sensitivity to its surrounded electrostatics (i.e., the electrostatic gating) [12–15]. However, as any electronic nanodevice, the ultrascaled JL CNTTFET suffers from some weaknesses, namely the low on-current and the issue of direct source-to-drain tunneling (DSDT), which is attributed to the low effective mass in the carbon nanotube [16–18]. Note that the DSDT phenomenon is the main cause in degrading the switching and subthreshold performance of CNT tunnel FETs in ultrascaled regime [18]. Recently, an ultrascaled CNTTFET with p-n doping profile has been proposed, showing spectacular improvements in terms of subthreshold and switching performance, including the on-current [18]. However, the p-n junction is still an intractable task even with the experienced progress in nanofabrication, including the doping techniques. A negative-capacitance carbon-nanotube-tunnel field-effect transistor (NC CNTTFET) has also been proposed recently through a quantum simulation study, where improved on-current was recorded by dint of ferroelectric-induced amplified inner-gate voltage [19]. However, the instability in NC-FET is still a concern. Moreover, the heterogeneous structure has been found as an intriguing approach to improve the on-current of CNTTFET with carbon nanotube-GNR heterojunctions [20]. However, the accurate realization of such an atomistic heterojunction is complicated and budget consuming, which is a concern. Therefore, new innovative techniques and simple improvement approaches should be developed while considering the fabrication aspect and TFET performance.

In this computational work, an efficient approach based on the synergy of electrostatic and chemical-doping engineering is proposed to boost the subthreshold and switching performance of sub-10 nm junctionless-carbon-nanotube-tunnel field-effect transistors. The proposed viable approach has been found to be very efficient in shrinking the band-to-band tunneling (BTBT) window and dilating the DSDT barrier, while boosting the subthreshold and switching performance of ultrascaled JL CNTTFET. The improved characteristics include the on-current, off-current, current ratio, subthreshold swing, leakage current, ambipolar behavior, I_{60} factor, power-delay product, and intrinsic delay. The proposed design has also shown high-performance in ultrascaled regime (with 5-nm gate length), where the sub-thermionic SS and high current ratio have been within reach.

The rest of this article is structured as follows. Section 2 details the proposed TFET structure. Section 3 summarizes the quantum simulation approach. Section 4 is devoted to present and discuss the results. Section 5 contains the conclusion.

2. Device Structure

Figure 1a shows the three-dimensional (3D) structure of the junctionless-carbon-nanotube-tunneling field-effect transistor (JL CNTTFET). The shape of the nanodevice follows the cylindricity of the carbon-nanotube channel, and, thus, coaxial gates are considered accordingly. Note that the gate-all-around (GAA) configuration is found to be more efficient in terms of controlling the carrier transport [21,22]. In addition, the GAA

structure really supports the assumption of uniform electrostatics in radial direction, thus making the simulation less complex [22]. In this work, a small CNT diameter was used, due to its appropriateness in terms of device electrical performance. Figure 1b shows the lengthwise-cut view of the uniformly doped JL CNTTFET. As shown, the tunneling FET is endowed with an auxiliary gate (P-gate) to electrostatically p-type dope the source side in order to preserve the junctionless aspect on CNT channel while achieving the tunneling FET operating regime [9]. As we can see, the control-gate at the middle of the device governs the FET carrier transport, while the drain side is left undoped. The Hafnium oxide (HfO_2) is considered to be a gate dielectric surrounding the zigzag CNT (Z-CNT). Figure 1c shows the doping profile of the conventional JL CNTTFET, which is uniformly n-type doped from source to drain electrodes. Figure 1d shows the cross-sectional view of the proposed engineered doping (ED)-based design, EDJL CNTTFET. As shown, this latter design is similar to the baseline design shown in Figure 1b, with the exception of three differences. The first is a heavily n-type doped pocket (HDP), which is located between the two coaxial gates with α concentration [23], the second is a lightly n-type doped portion (LDP) near the drain with β concentration, and the third is an electrical p-type doping gate with a tunable applied bias that aims to match the synergy. Figure 1e shows the doping profile of the proposed JL CNTTFET, showing the heavily n-type doped pocket between the P-G and C-G gates and the LDP near the drain electrode. From a fabrication point of view, the proposed non-uniform doping profile can be reached by tuning the exposure time of the concerned CNT portions to the employed chemical dopant and thus varying the doping level as required [13,22].

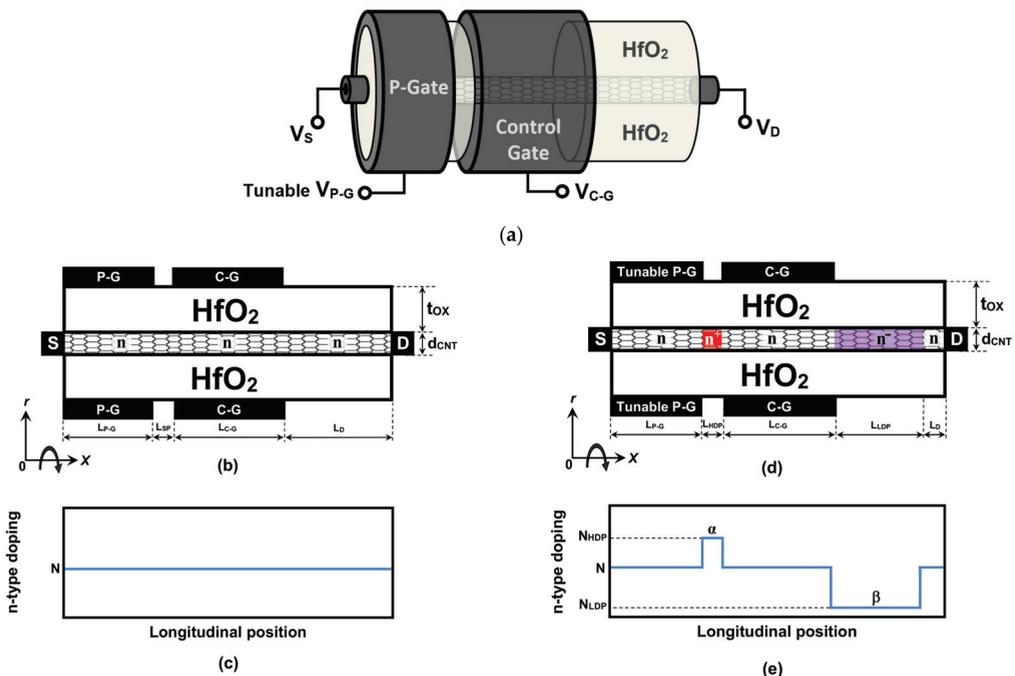


Figure 1. (a) Three-dimensional structure of the JL CNT tunneling FET. (b) Lengthwise-cut view and (c) doping profile of the conventional uniformly n-type doped JL CNT tunnel FET. (d) Lengthwise-cut view and (e) doping profile of the proposed non-uniformly n-type doped JL CNT tunnel FET with tunable P-G voltage.

All physical, electrical, and geometrical design parameters are shown in Table 1. Note that the physical backgrounds and reasons for the adopted chemical and electrical doping and their locations are discussed thoroughly in Section 4.

Table 1. Simulation parameters.

Parameter	Symbol	Value	Unit
Common parameters			
Z-CNT	$(n,0)$	10	-
Gap energy	E_G	~ 1.053	eV
CNT diameter	d_{CNT}	~ 7.82	Å
Gate length	$L_{\text{C-G}}$	10	nm
Drain length	L_D	10	nm
P-gate length	$L_{\text{P-G}}$	8	nm
Space between gates	L_{SP}	2	nm
S/C/D doping (CJL)	N	1	nm^{-1}
Oxide thickness	t_{OX}	1.5	nm
HfO ₂ dielectric constant	ϵ_{OX}	16	-
Temperature	T	300	K
Source gate voltage	$V_{\text{P-G}}$	-0.8	V
Drain-to-source voltage	V_{DS}	0.4	V
Additional parameters in the proposed design			
Heavily doped pocket	N_{HDP}	3	nm^{-1}
HDP Length	L_{HDP}	2	nm
Lightly doped pocket	N_{LDP}	$N/8$	nm^{-1}
LDP Length	L_{LDP}	7.5	nm

3. Simulation Approach

In the literature, the common quantum simulation method used to propose, investigate, and assess advanced nanoscale CNTFETs with full soundness and high accuracy is the self-consistent computation between the non-equilibrium Green's function formalism and the Poisson equation [22–25]. The main assets of this quantum simulation method are its ability to consider most of electrostatic features and the main quantum transport phenomena, including the band-to-band and direct source-to-drain tunneling mechanisms [22–26]. For this reason, we adopted the NEGF simulation in the present computational work. The retarded Green's function is the main equation on which this quantum simulation is based, and it can be expressed in the following matrix form [26]

$$G(E) = [(E + i\eta^+)I - H_{pZ} - \Sigma_S - \Sigma_D]^{-1} \quad (1)$$

where E , η^+ , H_{pZ} , I , and $\Sigma_{S(D)}$ are the energy, infinitesimal positive value, Hamiltonian matrix based on the atomistic nearest neighbor p_Z -orbital tight-binding approximation, identity matrix, and the source (drain) self-energy, respectively. In our computation, the mode space (MS) representation is employed to avoid the computational burden while considering only the relevant modes and the ballistic limit conditions [27]. Note that the source (drain) self-energy is analytically computed in accordance with the MS computational fashion [22,27]. The computation of the retarded Green's function and the S/D self-energies allows us to compute the source (drain) local density of states (LDOS), $D_{S(D)}$, using the following expressions [22]

$$D_{S(D)} = G\Gamma_{S(D)}G^\dagger \quad (2)$$

with

$$\Gamma_{S(D)} = i(\Sigma_{S(D)} - \Sigma_{S(D)}^\dagger) \quad (3)$$

where $\Gamma_{S(D)}$ denotes the energy level broadening due to the S/D contact. Now, the channel charge density is within reach, using the following equation [22]:

$$Q(x) = (-q) \int_{-\infty}^{+\infty} dE \cdot \text{sgn}[E - E_N(x)] \times \{D_S(E, x) f(\text{sgn}[E - E_N(x)](E - E_{FS})) + D_D(E, x) f(\text{sgn}[E - E_N(x)](E - E_{FD}))\} \quad (4)$$

where q , sgn , E_N , f , and $E_{FS(FD)}$ are the electron charge, sign function, charge neutrality level, Fermi function, and S/D Fermi level, respectively. In the self-consistent computation, computing the charge-density Equations (1)–(4) needs information on the on-site electrostatic potential, which is approximated by solving the Poisson equation for cylindrical nano-FET structure given by the following equation [22,27]:

$$\nabla^2 U(x, r) = -\frac{\rho(x, r)}{\epsilon} \quad (5)$$

where U , ϵ , and ρ are the potential distribution, the dielectric constant, and the Z-CNT charge density, including the chemical doping concentration, respectively. The Poisson equation is solved by using the finite difference method, while assuming that the potential is invariant in the coaxial direction. The Dirichlet boundary conditions are imposed on the gates' nodes, considering the relevant biases, while the Neumann boundary conditions are considered for the remaining external interfaces, including the source and drain electrodes [22,27]. After attaining the self-consistency between the Poisson solver and the MS NEGF solver, the drain current is within reach by using the following equation [22]:

$$I = \frac{4q}{\hbar} \int_{-\infty}^{+\infty} dE T(E) [f(E - E_{FS}) - f(E - E_{FD})] \quad (6)$$

where \hbar is the Planck's constant, and $T(E)$ is the transmission coefficient, which can be computed as follows [22]:

$$T(E) = \text{Tr} \left[\Gamma_S G \Gamma_D G^\dagger \right] \quad (7)$$

where Tr denotes the trace operator. All NEGF simulations were performed by using MATLAB software. For more information and details regarding the NEGF-based quantum mechanical simulation of nanoscale carbon-nanotube FETs, we refer to our previous relevant works [24,25,28,29], where the validation of the used NEGF simulation against some experimental and theoretical data was reported.

4. Results and Discussion

The nanoscale tunneling FETs are promising nanodevices, due to their assets, namely sub-thermionic subthreshold swing, low-off current, and intriguing scaling capability. However, the low on-current is considered the main disadvantage in these promising nano-FETs. Thereafter, we show interesting improvements in on-current, off-current, and subthreshold swing, using the synergy of both chemical and electrical-doping techniques, while keeping the junctionless paradigm. Figure 2a shows how the increase in doping concentration of the heavily n-type doped pocket boosts the on-current of the JL CNTTFET. When inspecting the same figure, we can observe that the off-current is also slightly improved with the N_{HDP} increase. The recorded off-current (on-current) improvement is principally attributed to the dilation (shrinking) in the DSdT (BTBT) window induced by the heavily doped pocket. Figure 2b shows that the recorded improvement in on-current, using the heavily doped pocket, can be further enhanced by increasing negatively the applied voltage of the auxiliary p-gate that ensures the source p-type doping electrostatically. We can also see that a slight increase in off-current is recorded, while the ambipolar behavior is still the same. The recorded additional improvement in on-current is logically attributed to an additional shrinking in the BTBT window that is induced by the negatively high

p-gate voltage. Therefore, in order to increasingly boost the on-current, it is appropriate to combine the HDP technique with that of the negatively high p-gate voltage.

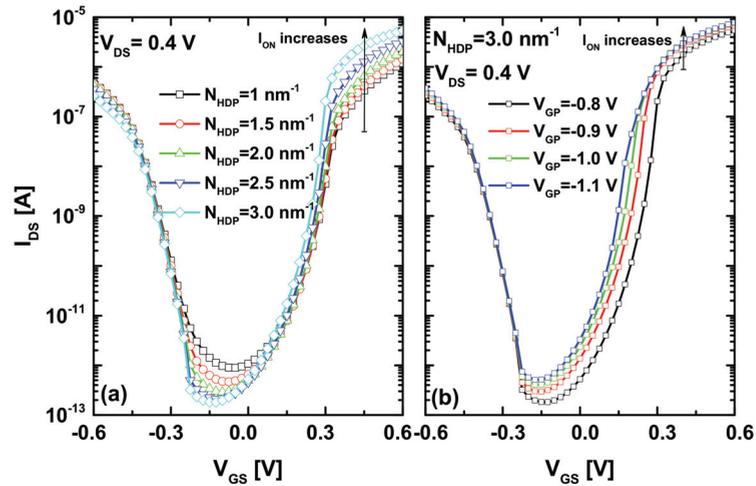


Figure 2. (a) Impact of doping concentration of the heavily n-type doped pocket between gates on the I_{DS} - V_{GS} transfer characteristics of JL CNTTFET. (b) Impact of P-gate voltage on the improved I_{DS} - V_{GS} transfer characteristics of JL CNTTFET endowed with HDP.

In order to decrease the off-current (increased with increasing the negative p-gate voltage as shown in Figure 2b) and improve the subthreshold swing, we adopted, in addition, a lightly doped portion to dilate the direct source-to-drain tunneling window, while keeping the junctionless paradigm. As expected, Figure 3a explicitly shows significant improvements in terms of on-current, off-current, subthreshold swing, and ambipolar behavior, in comparison to the conventional JL CNTTFET. We can clearly see the steep switching of the transfer characteristic, which is a highly desired feature in cutting-edge high-performance digital applications. Figure 3b shows the subthreshold swing in function with the drain current for the conventional and proposed nanoscale TFETs. This indicates that the drawn curves are important and informative, because they reveal the minimum SS on the one hand and the values of SS over the transfer characteristics on the other hand. The same figure also highlights the I_{60} factor, which denotes the highest drain current at which $SS = 60$ mV/dec is recorded. Note that the ideal region of the I_{60} metric in the plot is on the lower right corner, with a steep SS and high drain currents [30]. As shown, the performance of the proposed design is closest to the aforementioned region of interest, with a higher I_{60} factor in comparison to the baseline TFET. In addition, the proposed JL-CNTTFET exhibits a steeper SS than the conventional TFET over the considered I_{DS} range, and, thus, the average SS of the proposed JL-CNTTFET is smaller than that of the conventional one. It is worth noting that the proposed (conventional) design provides a minimum SS value of ~ 19 mV/dec (~ 33 mV/dec), as indicated in Figure 3a.

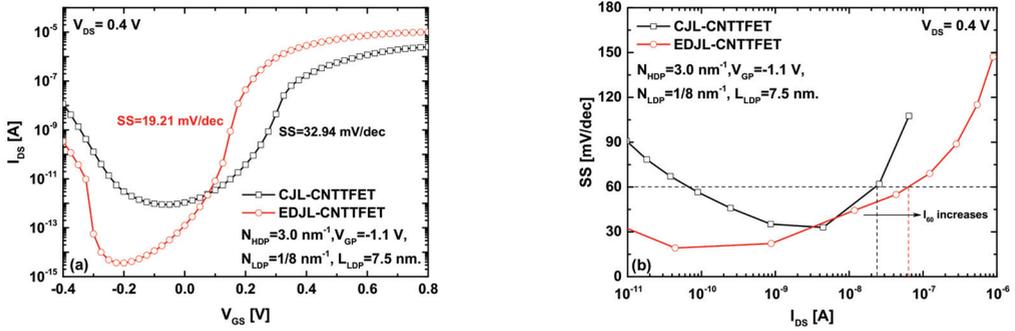


Figure 3. (a) I_{DS} - V_{GS} transfer characteristics of the conventional JL CNTTFET and the proposed JL CNTTFET, which includes the heavily n-type doped pocket, the optimized p-gate voltage, and the LDP near the drain electrode. (b) Subthreshold swing as a function of drain current for the standard and proposed nano-TFET.

Figure 4 shows the potential distribution drawn from the converged Poisson’s solutions at the lengthwise-cut region. The electrostatic gating of the p-gate and the main gate is clearly seen. More important, we can see in Figure 4a that the longitudinal potential variation between the two aforementioned electrostatic-gating examples (at the level of the ungated region, framed by a discontinued line) is somewhat wide, while reflecting the long BTBT window responsible for the low on-current. However, by using the V_{PG} adjustment and heavily n-type doped pocket, we can observe a steep longitudinal potential variation at the BTBT region, as shown in Figure 4b. In this latter example, it is also clearly seen the dilation in the DSDT window that is induced by the lightly n-type doped portion near the drain, making the nano-TFET more immune to the DSDT leakage, contrary to the conventional case.

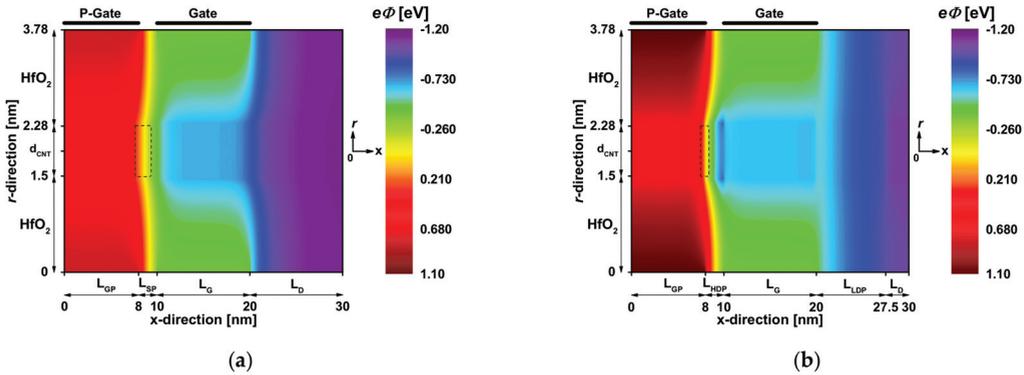


Figure 4. Two-dimensional potential distribution at $V_{GS} = 0.4 \text{ V}$ and $V_{DS} = 0.4 \text{ V}$ for (a) the CJL CNTTFET and (b) the proposed JL CNTTFET with chemical- and electrical-doping engineering.

Figure 5 shows how the band diagrams are tuned by using the chemical- and electrical-doping techniques in order to improve the low on-current, which is among the main drawbacks in nanoscale TFETs. In Figure 5, the top (bottom) solid line is the edge of conduction (valence) band edge, E_C (E_V). We can clearly see in all figures that the edge of the conduction band underneath the gate is below the edge of the source valence band, while allowing a band-to-band tunneling mechanism that results in the on-current in tunneling FETs. This indicates that the direct source-to-drain tunneling can also contribute to the BTBT on-current, especially in TFET with ultra-scaled gate lengths, where the DSDT

leakage becomes a concern. In Figure 5a, we can clearly see that the BTBT window indicated by two arrows is somewhat long, leading to low TFET on-currents. In Figure 5b, we can see the HDP-induced band lowering, which shrinks the BTBT window while increasing the BTBT components and making the on-current higher, as shown in Figure 2a. It is worth noting that the shorter (longer) BTBT window provides a higher (lower) on-current [18]. The inspection of Figure 5b also reveals a slight dilation in the DSDT window, due to the HDP-induced band lowering, while also explaining the recorded decrease in off-current shown in Figure 2a. Figure 5c shows that the BTBT window becomes somewhat shorter by increasing the p-gate voltage, and, thus, the BTBT on-current is boosted accordingly. Note that the negative increase in p-gate voltage also decreases the DSDT window, leading to the increase in off-current, as recorded in Figure 2b. For more clarification, Figure 5d is plotted to graphically show how the synergy of the HDP-based technique and the P-G voltage adjustment increasingly shrinks the BTBT window responsible for the on-current increase. In fact, the negative increase in P-gate voltage induces a band elevation at the level of source region, as shown in the same figure. Therefore, geometrically, the V_{PG} adjustment-induced band elevation, together with the HDP-induced band lowering, shrinks the BTBT window more and more, making it shorter, while clearly explaining the additional increase in on-current recorded in Figure 2b.

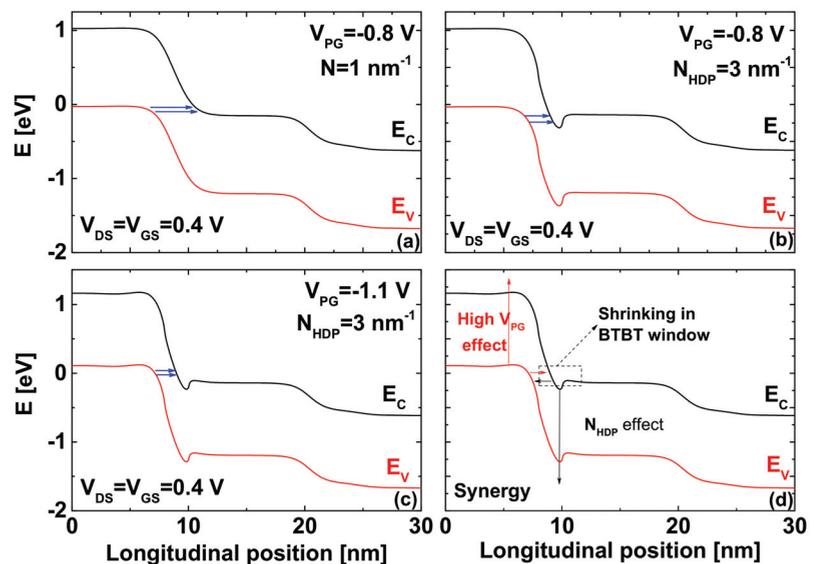
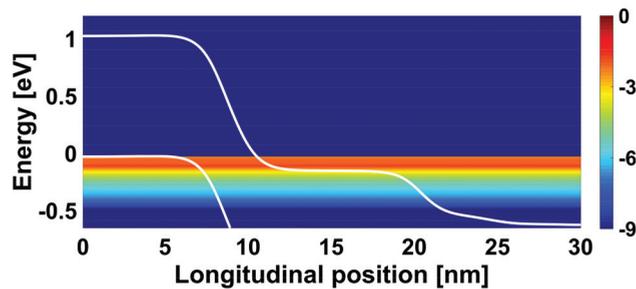
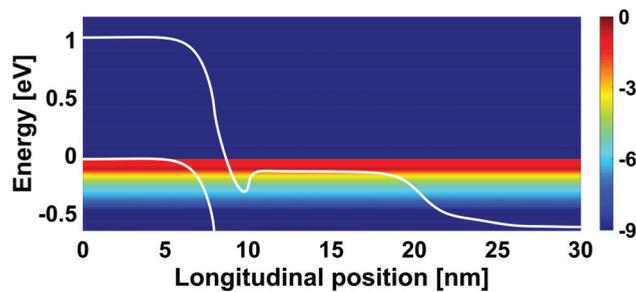


Figure 5. Band diagrams drawn at the on-state condition of (a) CJL CNTTFET, (b) JL CNTTFET with heavily n-type doped pocket, and (c) JL CNTTFET with both highly n-type doped pocket and optimized P-G voltage. (d) Doping-induced shrinking in BTBT window.

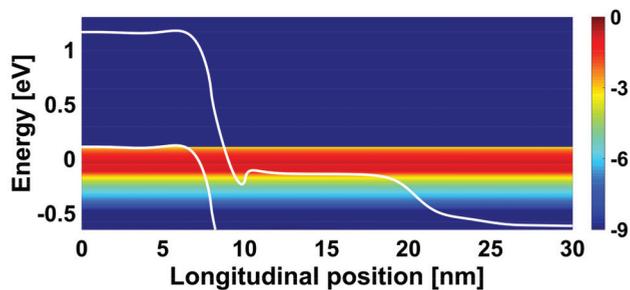
Figure 6 shows the energy-position-resolved current spectrum drawn from the NEGF quantities for the JL CNTTFETs under investigation. We can see in Figure 6a the band-to-band tunneling from source valence band to the drain conduction band through the BTBT window. In Figure 6b, we can clearly see that the BTBT on-current spectrum becomes higher than that of conventional JL CNTTFET, due to the HDP-induced band lowering that shrinks the BTBT window. Figure 6c obviously shows that the synergy of the p-gate voltage adjustment and heavily doped pocket approaches causes an additional increase in BTBT on-current spectrum (in comparison to other cases), due to the recorded additional shortening in BTBT window, as previously explained and shown in Figure 5.



(a)



(b)



(c)

Figure 6. Energy-position-resolved current spectrum at on-state ($V_{GS} = 0.4$ V and $V_{DS} = 0.4$ V) of (a) the CJL CNTTFET, (b) the JL CNTTFET with heavily n-type doped pocket, and (c) JL CNTTFET with both HDP ($N_{HDP} = 3 \text{ nm}^{-1}$) and optimized p-gate bias ($V_{PG} = -1.1$ V).

Figure 7 shows the role of the lightly n-type doped ZCNT region near the drain in dilating the direct source-to-drain tunneling window responsible for the tunneling leakage current in ultrascaled TFETs. As shown in Figure 7a, the DSDT window of the JL CNTTFET without the lightly n-type doped pocket is somewhat short (~ 14 nm), leading to a higher leakage current or, equivalently, a higher DSDT current; thus, a high off-state is recorded, as shown previously in Figure 2. Figure 7b clearly shows the LDP-induced dilation in the DSDT window by elevating the concerned bands via the lightly doped pocket. Please note that this LDP-induced dilation in the DSDT window explains the recorded improvement well in the off-current, I_{60} factor, and sub-thermionic subthreshold swing, as shown above in Figure 3.

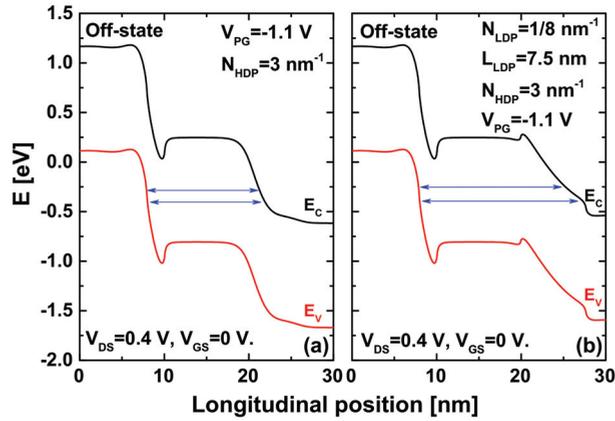


Figure 7. Band diagrams at the off-state for (a) JL CNTTFET with HDP and optimized V_{PG} ; and (b) JL CNTTFET endowed with HDP, optimized V_{PG} , and lightly n-type doped ZCNT portion near the drain electrode.

Figure 8a shows the electron-density distribution throughout the JL CNTTFET, without considering the lightly n-type doped pocket near the drain electrode. We can see that the direct source-to-drain tunneling window is somewhat short; equivalently, the source and drain reservoir are close, thus leading to a significant DSDT mechanism and a high leakage current spectrum, as shown in Figure 8b. Figure 8c shows the electron density per unit energy versus the longitudinal position at off-state for the JL CNTTFET, considering the LDP near the drain electrode. As shown, the source and drain reservoirs diverge, making the DSDT window longer, and, thus, a decrease in DSDT off-current spectrum is recorded, as shown in Figure 8d.

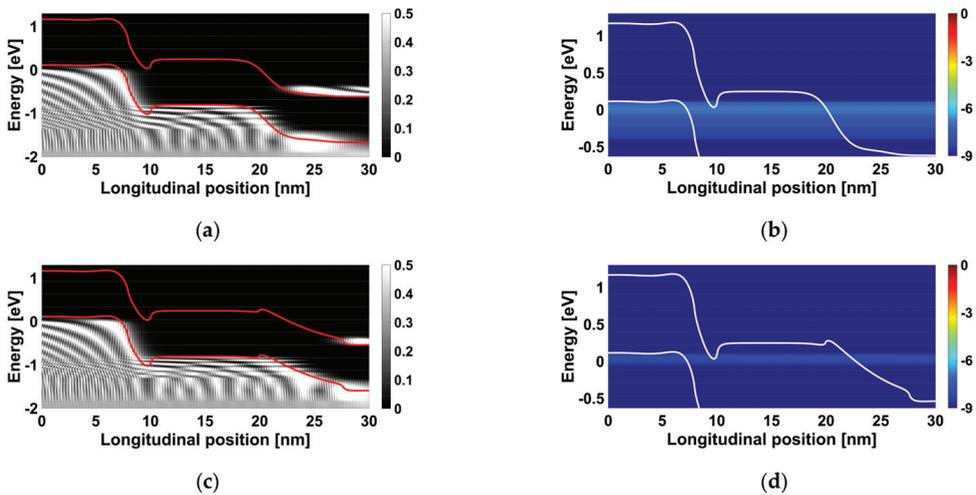


Figure 8. Electron density per unit energy versus the longitudinal position at off-state ($V_{GS} = 0$ V and $V_{DS} = 0.4$ V) for the JL CNTTFET (a) without and (c) with ($L_{LDP} = 7.5$ nm and $N_{LDP} = 1/8$ nm⁻¹) the lightly n-type doped portion near the drain electrode. Energy-position-resolved current spectrum for the JL CNTTFET (b) without and (d) with ($L_{LDP} = 7.5$ nm and $N_{LDP} = 1/8$ nm⁻¹) the LDP near the drain electrode.

Figure 9a shows how the decrease in doping concentration of the lightly n-type doped pocket near the drain improves the subthreshold swing and off-current and suppresses the ambipolar behavior. It is worth noting that we have not considered very low doping concentrations in order to keep the junctionless paradigm and avoid the n-type doping-intrinsic abrupt junction. The recorded improvements are attributed to the light doping-induced band elevation that dilates the DSDT window. In Figure 9b, the same improvement behavior is recorded when increasing the length of the LDP, where enhancements in terms of sub-thermionic subthreshold swing, off-current, and ambipolar behavior are recorded, while optimized on-current is within reach by the chemical and electrical-doping techniques near the source, as shown above. Therefore, wide lightly n-type doped ZCNT portions with a low concentration are suitable for improved subthreshold performance; however, there are some considerations regarding the junctionless aspect, the scaling capability, and the ohmic drain contact.

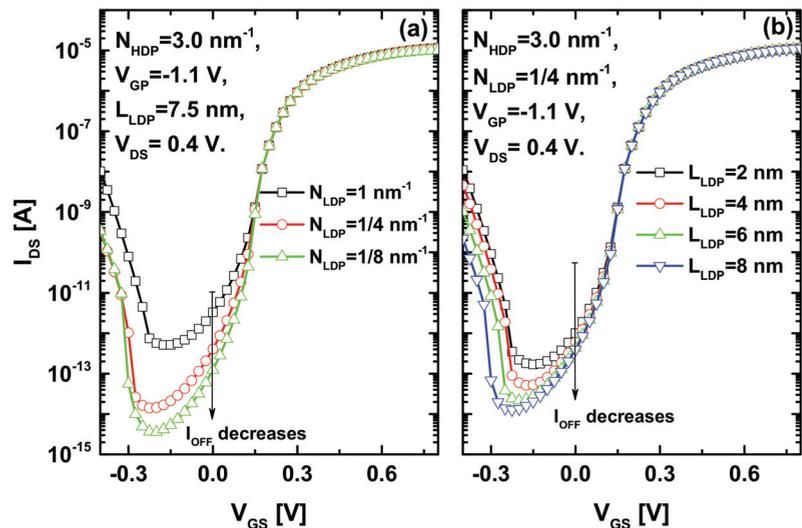


Figure 9. Impact of (a) doping concentration of the lightly n-type doped pocket near the drain and (b) the length of LDP on the I_{DS} - V_{GS} transfer characteristics of the proposed JL CNTTFET.

Figure 10 shows the switching performance of the conventional and proposed nanoscale TFETs, including the off-current (I_{OFF}); on-current (I_{ON}); current ratio (I_{ON}/I_{OFF}); power-delay product, $PDP = (Q_{ON} - Q_{OFF})V_{DD}$; and the intrinsic delay, $\tau = (Q_{ON} - Q_{OFF})/I_{ON}$. It is to indicate that the intrinsic delay presents how fast the JL CNTTFET can switch, while the power-delay product shows the energy required for a switching event. Note that the curves in Figure 10 are drawn from the concerned transfer characteristics by shifting a switching window with a width of power-supply voltage (V_{DD}) equal to 0.4 V, while extracting the on-state total charge (Q_{ON}) and its current (I_{ON}) at each given V_{GS-ON} , and the corresponding off-state total charge (Q_{OFF}) and its current (I_{OFF}) at $V_{GS-OFF} = V_{GS-ON} - V_{DD}$ [31–33].

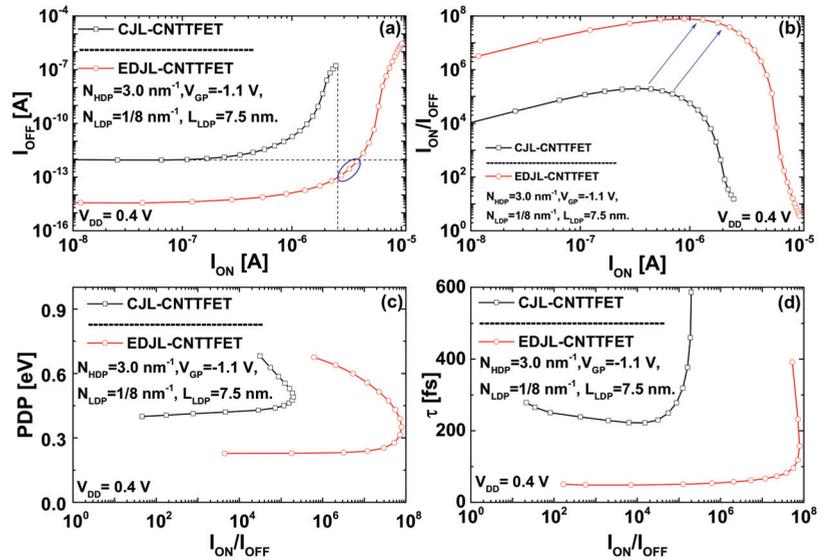


Figure 10. (a) Off-current versus on-current, (b) I_{ON}/I_{OFF} current ratio in function of the on-current, (c) power delay product as a function of current ratio, and (d) intrinsic delay versus the I_{ON}/I_{OFF} current ratio for the conventional and proposed JL CNTTFETs.

Figure 10a shows that the proposed JL CNTTFET can provide higher (lower) on-current (off-current) for a shared off-current (on-current) in comparison with the conventional nanodevice. Our inspection of the same figure reveals that the proposed JL CNTTFET, which is endowed with electrical- and chemical-doping engineering, can provide a particular performance (highlighted by a solid circle), where both higher on-current and lower off-current were simultaneously recorded in comparison with the currents of the conventional JL CNTTFET. Figure 10b is drawn from the concerned transfer characteristics, showing that the proposed JL CNTTFET can exhibit a higher maximum reachable current ratio (MRCR) with higher on-current, as indicated by arrows. Note that the MRCR of the proposed device is higher than that of the conventional device by about three orders of magnitude. In addition, we can clearly see that the proposed device exhibits a higher I_{ON}/I_{OFF} current ratio than the conventional device over the shared range of on-currents. Figure 10c shows and compares the power-delay product (PDP) in function of I_{ON}/I_{OFF} current ratio for the proposed and conventional JL CNTTFET. It is clearly seen that the proposed nanodevice exhibits lower PDP (higher I_{ON}/I_{OFF}) than its conventional counterpart over the shared range of current ratio (PDP). In addition, we can observe that the proposed device exhibits a higher MRCR with a lower PDP than that of the CJL CNTTFET. The recorded improvements in terms of PDP empower the proposed design to be an intriguing energy-efficient nano-TFET for high switching applications. Figure 10d shows that the proposed device provides faster (higher) intrinsic delay (current ratio) than its conventional counterpart over the shared range of current ratio (intrinsic delay). In addition, we can also see that the proposed design provides higher MRCR with faster delay than that of the CJL CNTTFET. The substantial decrease in terms of intrinsic delay, together with the recorded current ratios, makes the proposed JL CNTTFET an interesting nanoscale junctionless tunnel FET for high-speed applications.

In order to assess the benefits of the proposed design in the ultrascaled regime, we have performed a quantum-simulation-based comparison between the conventional and the proposed nanodevices, considering the main parameters of switching performance. Table 2 summarizes the main switching figures of merit of the proposed JLCNTTFET with 5

nm gate length. As very interesting results, the current ratio is improved by about 3 orders of magnitude and sub-thermionic SS (43 mV/dec) is well recorded in ultra-scaled regime. In addition, the on-current is boosted, and the off-current, minimum leakage current (I_{MIN}), I_{60} factor, PDP, and intrinsic delay are all decreased, which is very important for high-speed, low-power, and high-performance switching applications.

Table 2. Switching performance of JL CNTTFETs with 5 nm gate length.

Parameter	CJL-CNTTFET	EDJL-CNTTFET
I_{ON} (A)	7×10^{-7}	1.34×10^{-6}
I_{OFF} (A)	3.4×10^{-9}	1.23×10^{-11}
I_{MIN} (μA)	1.41×10^{-3}	2.05×10^{-6}
I_{60} (A)	-	5.6×10^{-8}
$I_{\text{ON}}/I_{\text{OFF}}$	205.8	10^5
SS (mV/dec)	128	43
PDP (eV)	0.52	0.31
τ (fs)	300.8	94.3

Basing on the recorded results in terms of the on-current improvement, which is attributed to the doping-induced shrinking in BTBT window, the ferroelectric-based gating can be adopted as additional improvement approach in order to further improve the EDJL-CNTTFET performance via the feature of the FE-induced amplified gate voltage [34], and thus well exploiting the boosted BTBT on-current. In fact, the adoption of ferroelectric (FE) material can take two different designs. The first configuration is based on the metal-ferroelectric-insulator-semiconductor (MFIS) design, while the second arrangement is the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [35]. We adopt in our case the MFMIS configuration due to its benefits in terms of elaboration [35–37], the possibility of separate integration [38], and the simulation simplicity [39–41]. Figure 11a shows an EDJL-CNTTFET design with a MFMIS structure. Note that the MFMIS can be integrated as a coaxial gate [42] or used as separate gating system ideally connected by a wire [25,38,41,43]. From simulation point of view, the ferroelectric field-effect transistors endowed with a MFMIS system can be treated as a baseline field-effect transistor in series with a ferroelectric capacitor [25,40–44]. Therefore, conceptually, the numerical modeling of the negative capacitance (MFMIS) nanodevices is divided into two parts [45]. The first step of simulation deals with the baseline device as mentioned above in the Section 3. After the self-consistency, the gate charge (Q_G) is numerically extracted and used to compute the voltage across the FE material (V_{FE}), using the 1-D steady-state Landau–Khalatnikov equation, which is given as follows [34]:

$$V_{FE} = 2\alpha t_{FE} Q_G + 4\beta t_{FE} Q_G^3 + 6\gamma t_{FE} Q_G^5 \quad (8)$$

where t_{FE} is the FE thickness; and (α , β , and γ) are the FE Landau coefficients, which are chosen to be as those of the Al-doped HfO_2 FE parameters [25,44–46]. After computing V_{FE} , the external gate voltage (V_{GS}) of the EDJL-CNTTFET is normally computed by using the following equation [25,39–45]:

$$V_{GS} = V_{INT} + V_{FE} \quad (9)$$

where V_{INT} is the internal metal-gate voltage considered in the baseline self-consistent quantum simulation. For more computational information regarding the quantum simulation of ultrascaled MFMIS FE-FETs, we refer the reader to our previous works [19,25,45].

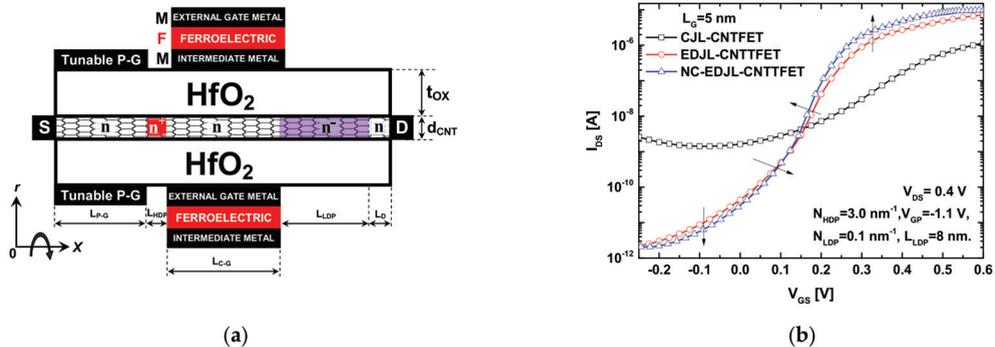


Figure 11. (a) Cross-sectional view of the proposed NC-EDJL-CNTTFET with MFIS structure. (b) I_{DS} - V_{GS} transfer characteristics of the conventional JL CNTTFET, the proposed EDJL-CNTTFET, and the proposed NC-EDJL-CNTTFET considering 5 nm gate length.

Figure 11b shows that the proposed electrical- and chemical-doping approach can significantly improve the I_{DS} - V_{GS} transfer characteristics of an ultrascaled JL CNTTFET with 5 nm gate length. We can clearly see the substantial improvements in terms of I_{ON} , I_{OFF} , current ratio, and leakage current. In addition, we can observe that the nanodevice with the MFIS structure additionally improves the on-current, off-current, and subthreshold swing, due to the FE-induced amplified gate voltage. Note that the recorded subthreshold swing recorded in EDJL-CNTTFET was decreased from 43 to 35 mV/dec via the FE-based improvement approach. This indicates that the adoption of more appropriate FE nanomaterial with particular coercive field and remnant polarization can increasingly boost the nanodevice performance via enhancing the FE-induced amplified internal gate voltage [45]. In order to find the best device and ferroelectric parameters that can lead to the ultimate best performance, a parametric investigation [47] based on metaheuristic techniques (e.g., ant colony optimization, practical swarm optimization, genetic algorithms [48], etc.) in conjunction with the used NEGF simulation approach can be followed, while solving an advanced optimization problem, which can be a matter for future investigations.

The intriguing results obtained in this computational work can give new impulses to the design, simulation, and optimization of the advanced 2D materials-based nanoscale FETs with ultra-thin dielectrics, which have experienced significant progress [49–57]. In addition, the employment of such intriguing steep-slope nanodevices in advanced sensing applications [48,58–61] can be a matter for future works.

5. Conclusions

In this article, a new approach based on the synergy of the electrostatic and chemical-doping engineering is proposed to boost the performance of nanoscale JL CNTTFETs. The hybrid doping approach was found to be efficient at shrinking the BTBT window and dilating the DSDT spacing, while also boosting the JL CNTTFET performance. The profound quantum transport investigations have included the band diagrams, the potential distributions, and the energy-position-resolved electron density and current spectra. As a result, the subthreshold and switching performance is significantly improved, where subthermionic subthreshold swing, mitigated ambipolar behavior, boosted on-current, higher current ratio, reduced off- and leakage-current, faster switching speed, lower switching power, and improved scaling capability were obtained. Moreover, the metal–ferroelectric–metal-based gating approach was employed in order to exploit the recorded improvement in carrier transport, while boosting the JL TFET switching performance. The proposed design based on the synergy of electrostatic and chemical-doping engineering solved the main problems in ultrascaled JL CNTTFETs, and this is promising for the future CNT-based nanoelectronics.

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Article

Area-Scalable 10^9 -Cycle-High-Endurance FeFET of Strontium Bismuth Tantalate Using a Dummy-Gate Process

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Abstract: Strontium bismuth tantalate (SBT) ferroelectric-gate field-effect transistors (FeFETs) with channel lengths of 85 nm were fabricated by a replacement-gate process. They had metal/ferroelectric/insulator/semiconductor stacked-gate structures of Ir/SBT/HfO₂/Si. In the fabrication process, we prepared dummy-gate transistor patterns and then replaced the dummy substances with an SBT precursor. After forming Ir gate electrodes on the SBT, the whole gate stacks were annealed for SBT crystallization. Nonvolatility was confirmed by long stable data retention measured for 10⁵ s. High erase-and-program endurance of the FeFETs was demonstrated for up to 10⁹ cycles. By the new process proposed in this work, SBT-FeFETs acquire good channel-area scalability in geometry along with lithography ability.

Keywords: FeFET; ferroelectric; nonvolatile; semiconductor memory; SBT

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1. Introduction

Ferroelectric-gate field-effect transistors (FeFETs) comprising SrBi₂Ta₂O₉ (SBT) or Ca_xSr_{1-x}Bi₂Ta₂O₉ (CSBT) ferroelectrics have unique characteristics of high endurance against at least 10⁸ cycles of program and erase operations [1–12]. CSBT is a kind of SBT family which was derived from original SBT by Sr-site substitution with Ca. The material natures of SBT [13–32] and CSBT [33–36] have been intensively studied previously. FeFETs using CSBT with about $x = 0.2$ showed larger memory windows than those with SBT [5]. The invention of long-retention FeFET was first reported in 2002 and consisted of a metal/ferroelectric/insulator/semiconductor (MFIS) stacked-gate structure of Pt/SBT/(HfO₂)_{0.75}(Al₂O₃)_{0.25}(HAO)/Si [37]. Since then, we have investigated characteristics of (C)SBT-FeFETs [1–3,38–44], improved the device performance [4–8,45,46], and developed FeFET-integrated circuits [9–12,47–52]. For improving the single FeFET performance, we succeeded in reducing gate voltage (V_g) from the initial 6–8 [1] to 3.3 V [8]. Another progress was in shrinking gate-metal length (L_m) from the initial 10 μ m [1] to 100 nm [7].

The conventional (C)SBT-FeFETs were formed by etching the gate stacks. By decreasing the FeFET gate length, SBT etching-damage problems [29–32] on the gate-stack sidewalls became significant. Since we recognized that $L_m = 100$ nm was approaching the shortest limit by the conventional method based on etching, we changed the fabrication strategy to shape the gate stacks from etching-down to filling-up. The new (C)SBT-FeFET process is outlined as follows: Dummy-gate transistor patterns with self-aligned source- and drain regions are prepared in advance. The dummy substance is selectively removed to leave grooves which are later filled up with SBT precursor. Gate electrodes are formed. Finally, whole gate stacks of Ir/SBT/HfO₂/Si are annealed for SBT crystallization. In the new FeFET process, the (C)SBT sidewall of the gate stack is not exposed to etching plasma. The sidewall is thus free from etching damage problem [6]. Consequently, the ferroelectric becomes more controllable in terms of quality and more scalable in terms of geometry than by the etching. The new FeFET dimensions follow good lithography progress with an

adequate height of (C)SBT to show large memory windows increasing with the ferroelectric thickness [3,43]. In this work, SBT-FeFETs with gate channel lengths $L_{ch} = 85$ nm were first reported by adopting the proposed process. Excellent characteristics were demonstrated such as 10^9 cycle erase-program endurance and long stable retention for 10^5 s. The endurance and retention were as good as those of the conventional (C)SBT-FeFETs formed by the gate-stack etching [1–12].

2. Materials and Methods

2.1. Device Fabrication Process

The fabrication process (schematic drawings shown in Figure 1) in this work is as follows:

- *Step 1: Si substrate preparation.* A *p*-type Si substrate patterned with FET active areas was prepared. Local-oxidation-of-silicon (LOCOS) process was used in the patterning for device isolation. The LOCOS patterns with various channel widths (W) were designed in a sample chip. Areas for source-, drain- and substrate-contact holes on the Si were heavily ion-doped. Sacrificial SiO_2 on Si was removed with buffered hydrogen fluoride.
- *Step 2: Insulator deposition.* A 5 nm thick HfO_2 was deposited on the Si substrate by a large-area pulsed-laser deposition system (Vacuum Products Corporation, Kodaira, Tokyo, Japan) [53]. A KrF laser was irradiated on a ceramic HfO_2 target in 15.3 Pa N_2 ambient [54]. The substrate temperature was 220 °C.
- *Step 3: Lithography.* Electron-beam (EB) lithography was performed by spin-coating an organic resist, exposing 130 kV EB, and developing. Resist patterns 550 nm tall were left on the HfO_2/Si . They were later used as ion-implantation mask in *Step 4* and as dummy gates in *Step 7*.
- *Step 4: Ion implantation.* HfO_2 uncovered with resist was etched out by inductively-coupled-plasma reactive-ion etching (ICP-RIE). On the exposed Si, As^+ ions were implanted for source and drain. The energy and dose conditions were 4 keV and $5.0 \times 10^{12}/\text{cm}^2$.
- *Step 5: SiO_2 deposition.* An 830 nm thick SiO_2 was deposited to cover the resist patterns on the substrate by 300 W rf sputtering in 0.1 Pa Ar.
- *Step 6: Flattening SiO_2 .* The SiO_2 was etched back and flattened by ICP-RIE with 1.0 Pa Ar- CF_4 mixed gas until tops of the resists or dummy gates were exposed.
- *Step 7: Leaving grooves on gates.* The dummy-gate substances were selectively removed by O_2 plasma ashing. There remained grooves in a 410 nm tall SiO_2 isolation. The grooves were located on the HfO_2 with self-aligned source and drain regions prepared in *Step 4*. The whole chip was rapidly annealed at 800 °C in ambient N_2 .
- *Step 8: Ferroelectric deposition.* SBT precursor film was deposited to fill up the grooves by a metal-organic-chemical-vapor deposition (MOCVD) system (WACOM R&D, Nihonbashi, Tokyo, Japan). Sources of $\text{Bi}(\text{C}_5\text{H}_{11}\text{O}_2)_3$, $\text{Sr}[\text{Ta}(\text{OC}_2\text{H}_5)_5(\text{OC}_2\text{H}_4\text{OCH}_3)]_2$ and $\text{Ta}(\text{OCH}_2\text{CH}_3)_5$ (Tri Chemical Laboratories Inc., Uenohara, Yamanashi, Japan) were used [6]. As-deposited precursor-film thickness was estimated as 80 nm on a flat place of the substrate.
- *Step 9: Metal deposition.* Ir was deposited by rf sputtering on the SBT precursor layer. Resist mask was patterned for gate electrodes by EB lithography.
- *Step 10: Forming gate electrodes.* Ir uncovered with resist was etched out by Ar^+ ion milling. Then, the resist mask was removed by O_2 plasma ashing.
- *Step 11: FeFET completed.* SBT precursor was deposited again by MOCVD to cover the substrate [6]. The whole substrate was annealed for crystallization of the SBT to show ferroelectricity. The annealing condition was at 780 °C in an O_2 - N_2 mixed gas we investigated before [8]. Finally, contact holes for gate, source, drain and substrate were formed by ultraviolet g-line lithography and Ar^+ ion milling.

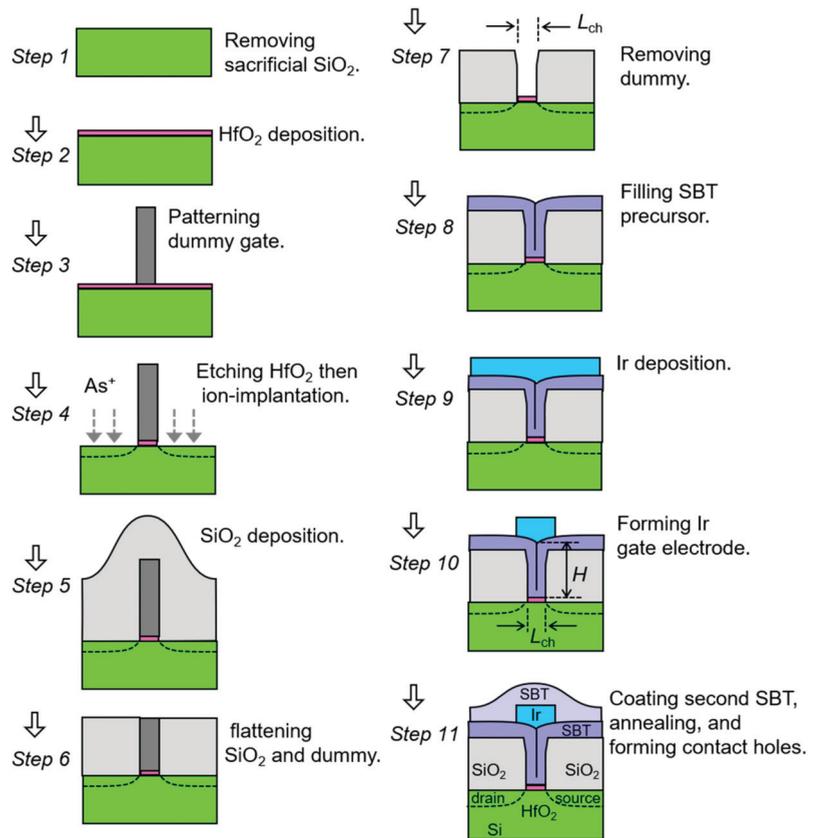


Figure 1. New fabrication process of Strontium bismuth tantalate (SBT)-ferroelectric-gate field-effect transistors (FeFETs) demonstrated in this work.

2.2. Reason for Using SBT in FeFET

The gate stack of MFIS should be regarded as MFI(IL)S, as shown in in Figure 2a, where F, I, IL, S are connected in series. The IL is an interfacial layer between I and S which is formed during the ferroelectric crystallization annealing process of FeFETs [8,39,55–57]. The main component of IL is silicon dioxide with an electric permittivity (ϵ_{IL}) of $\epsilon_{IL} = 3.9$. In the MFI(IL)S, $|P_F| \approx \epsilon_0 \cdot \epsilon_I \cdot |E_I| = \epsilon_0 \cdot \epsilon_{IL} \cdot |E_{IL}| = |Q_S|$ is satisfied in any time. The P_F is ferroelectric polarization. E_I and E_{IL} are electric fields in the I and the IL. The Q_S is charge area density in the semiconductor surface. The ϵ_I is a relative permittivity of the I. The ϵ_0 is the vacuum dielectric constant of $\epsilon_0 = 8.85 \times 10^{-12}$ F/m. For a simplified explanation, we assumed a virtual equivalent circuit of series capacitance as drawn in Figure 2a which is expressed by $|P_F| \approx |Q_I| \approx |Q_{IL}| = |Q_S|$ with virtual charges Q_I and Q_{IL} on I and IL, respectively. In MFI(IL)S, the IL suffers from a stress of field $|E_{IL}| \approx |P_F| / (\epsilon_0 \cdot \epsilon_{IL}) = 8.7$ MV/cm even at a small $|P_F| = 3 \mu\text{C}/\text{cm}^2$. For example, real IL thickness is 2.6 nm [8] or about 1 nm [55–57]. Electric-field-assisted tunnel current through such a thin SiO_2 [58,59] brings charge injection into the gate stack from S across IL. In erase-and-program operations, a large E_{IL} derived from a large P_F swing induces significant trapped-charge accumulation which accelerates endurance degradations [2,52]. According to our experience [43,52,60], $|P_F|$ should normally be less than $2.5 \mu\text{C}/\text{cm}^2$ all the time and should not exceed $2.0 \mu\text{C}/\text{cm}^2$ for further high-endurance requirements of the FeFET.

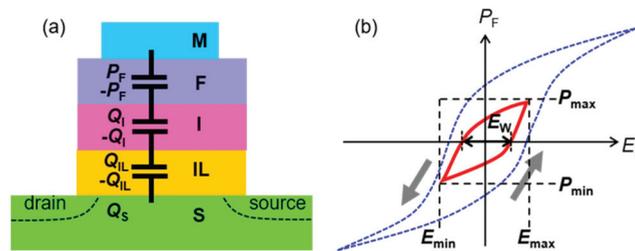


Figure 2. (a) Schematic cross-section of a FeFET with an equivalent circuit of MFI(IL)S gate stack. For convenience of explanation, the circuit is represented using virtual capacitances instead of a strict physical explanation by the electric flux density continuity, D . (b) Schematic drawings of P_F versus E_F . All P_F - E_F loops are drawn in counter-clockwise directions. The inner loop (red solid) is a minor loop corresponding to unsaturated P_F discussed in Section 2.2. Outer loop (blue broken) is a major loop for saturated P_F added as a reference. Every loop has its P_{\max} at E_{\max} and P_{\min} at E_{\min} .

Ferroelectric materials show P_F versus E_F hysteresis loops as illustrated in Figure 2b. The E_F is the electric field across the F. We defined E_{\max} as the positive maximum E_F and P_{\max} as the P_F at $E_F = E_{\max}$. Similarly, E_{\min} and P_{\min} are the negative minimum E_F and the P_F at $E_F = E_{\min}$. The loop is called “major” loop when the E_{\max} and $|E_{\min}|$ are strong enough to force P_F saturated, whereas it is called “minor” loop when P_F is unsaturated by moderate E_F swing. In SBT-FeFETs, restrictions of $P_{\max} \leq 2.5 \mu\text{C}/\text{cm}^2$ corresponding to the minor loops are used during all operations as we emphasized in early works [39,43,52,60].

Regarding a ferroelectric hidden in MFI(IL)S, an exact symmetric swing maximum, i.e., $P_{\max} = |P_{\min}|$ or $E_{\max} = |E_{\min}|$, is difficult because $|Q_S|$ versus Φ_S is very asymmetric [61,62]. The Q_S is the charge area density of the semiconductor surface and Φ_S is the surface potential. Presence of the flat-band voltage V_{fb} makes the symmetric swing further difficult. However, to simplify the physical explanation, $P_{\max} = |P_{\min}|$ and $E_{\max} = |E_{\min}|$ are assumed as shown in Figure 2b with $V_{fb} = 0\text{V}$. In every P_F - E_F loop, the E_F width at $P_F = 0$ is defined as E_w being related with a voltage memory window (V_w) by an approximate expression $E_w = 2E_c = V_w/d_F$, where the E_c is a coercive field and d_F is ferroelectric thickness. According to a method we proposed before [43], an important characteristic E_{\max} of the ferroelectric can be evaluated which has not been measurable by direct probing on a FeFET. If P_{\max} is provided, a gate voltage V_g to achieve a target memory window $V_w = E_w \cdot d_F$ can be estimated as a sum of $E_{\max} \cdot d_F$, $E_I \cdot d_I$, $E_{IL} \cdot d_{IL}$ and Φ_S at $Q_S = P_{\max}$. An exact discussion can be found in the paper [43].

For instance, Pt/SBT/HAO/Si FeFETs showed $E_w = 18 \text{ kV}/\text{cm}$ at $P_{\max} = 2.0 \mu\text{C}/\text{cm}^2$ and $E_{\max} = 25 \text{ kV}/\text{cm}$ [43]. By adopting an advanced process [8], Ir/CSBT/HfO₂/Si FeFETs had the best improved values of $E_w = 65 \text{ kV}/\text{cm}$ at $P_{\max} = 2.0 \mu\text{C}/\text{cm}^2$ and $E_{\max} = 140 \text{ kV}/\text{cm}$ [3,43]. A good reason for using (C)SBT in Si-based FeFETs is the (C)SBT ferroelectric nature of a convenient minor P_F - E_F loop [14,17,20] which has E_w available and is controllable in a restricted P_F range of $P_{\max} \leq 2 \mu\text{C}/\text{cm}^2$ with $E_{\max} \leq 140 \text{ kV}/\text{cm}$.

There are some other ferroelectric materials also intensively studied for applications in Si-based MFIS FeFETs. Regarding Pb₅Ge₃O₁₁ (PGO), attempts to develop replacement-type Pt/PGO/ZrO₂/Si FeFETs were reported [63] but the erase-program-test results of the FeFETs were not found although the ferroelectric itself showed a good potential P_{\max} - E_{\max} and $E_w - E_{\max}$ judging from hysteresis loops of the PGO metal/ferroelectric/metal capacitors [64]. Regarding another candidate, the ferroelectric HfO₂ family [55–57,65–70], the intrinsic material nature may not be suitable for applying to Si-based FeFETs. Informative minor hysteresis loops were reported on Y-doped HfO₂ in which E_w seemed nearly equal to 0 V/cm at $P_{\max} = 2.0 \mu\text{C}/\text{cm}^2$, although it was as large as about 1 MV/cm at $P_{\max} = 10 \mu\text{C}/\text{cm}^2$ [66]. Operation of the FeFETs under the restriction of $P_{\max} \leq 2 \mu\text{C}/\text{cm}^2$ may be difficult. Some reports suggested that HfO₂-FeFETs cannot help using a large P_{\max} ($>> 2 \mu\text{C}/\text{cm}^2$) [52,55]. The large P_{\max} may induce significant charge injection into the gate

stack. As far as we know, fair works on HfO_2 -FeFETs have not cleared 10^8 cycles endurance in spite of using sophisticated production facilities [56,67–70].

3. Results and Discussion

3.1. Device Dimensions

A cross-sectional scanning-electron-microscope photograph of an Ir/SBT/HfO₂/Si FeFET fabricated by the new proposed process is shown in Figure 3a. Figure 3b shows the same picture added with support lines to clarify the material boundaries. The schematic drawing of the FeFET was assigned with four terminals of gate, drain, source and substrate (Figure 3c). The gate-channel length (L_{ch}) was $L_{\text{ch}} = 85$ nm. The gate-channel width was $W = 100$ μm depending on the initial LOCOS pattern designed in Step 1 in Section 2.1. The metal-gate length L_{m} was 150 nm which could be shorter but was not the focus in this work. The SBT precursor film thickness was about 80 nm measured on a flat place. By filling gate grooves with SBT precursor (Step 8 in Section 2.1.), the effective SBT height (H) was finally about 450 nm which was a distance between Ir and HfO₂. Area scalability of the new FeFET was equivalent to that of the dummy gates which are organic resist patterns made by lithography. From the viewpoint of Si transistor technology, $L_{\text{ch}} = 10$ nm is expected to be the critical limit [71]. A significant Curie-temperature decrease in SBT started when particle were sizes of around 20 nm [25]. Thus, the prospective shortest limit of L_{ch} by our proposed FeFET process may be around 20 nm.

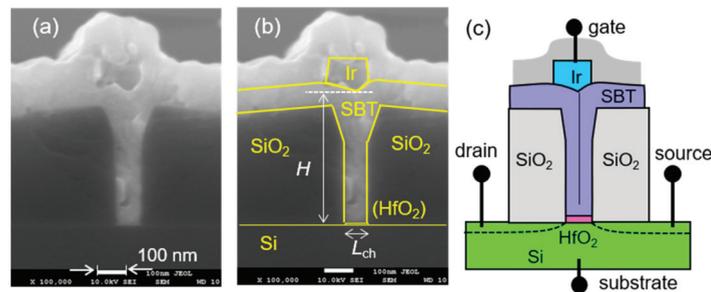


Figure 3. Cross-section of a FeFET with $L_{\text{ch}} = 85$ nm fabricated in this work. (a) Original photo by SEM observation and (b) the photo with supporting lines added to clarify material boundaries. (c) Schematic drawing assigned with gate, drain, source and substrate terminals for electrical characterizations.

3.2. Electrical Characterizations

In this study, memory windows, endurance and retention of FeFETs were investigated at room temperature. A semiconductor parameter analyzer (4156C, Keysight Technologies, Santa Rosa, CA, USA) was used for measuring static drain current versus gate voltage ($I_{\text{d}}-V_{\text{g}}$) curves of the FeFETs. A pulse generator (81110A, Keysight Technologies, Santa Rosa, CA, USA) was used to apply V_{g} pulses. The instruments were computer-controlled using programs written by the language of LabVIEW (ver. 10, National Instruments, Austin, TX, USA).

3.2.1. Memory Windows

As an elementary test of the FeFETs, $I_{\text{d}}-V_{\text{g}}$ hysteresis loops were investigated (Figure 4). The I_{d} was measured by V_{g} increments and decrements with 0.1 V steps. The V_{g} sweeping ranges were $V_{\text{g}} = 1 \pm 4$ V, 1 ± 5 V and 1 ± 6 V. Drain voltage (V_{d}), source voltage (V_{s}) and substrate voltage (V_{sub}) were fixed to $V_{\text{d}} = 0.1$ V and $V_{\text{s}} = V_{\text{sub}} = 0$ V during the measurements. The $I_{\text{d}}-V_{\text{g}}$ showed hysteresis loops drawn in counter-clockwise directions because the FeFET was an n -channel-type one. In an $I_{\text{d}}-V_{\text{g}}$ curve, threshold voltage (V_{th}) was defined as a V_{g} value at $I_{\text{d}}/W = 1 \times 10^{-7}$ A/cm. Two V_{th} values were extracted from the left- and right-side curves in an $I_{\text{d}}-V_{\text{g}}$ hysteresis loop. A memory window was defined

as the V_{th} difference. In this work, we call this a *static* memory window (V_w) because V_g sweep by 4156C is slow. The static V_w was, for instance, 1.0 V by sweeping V_g from -5 to 7 V then back to -5 V, or at $V_g = 1 \pm 6$ V as expressed in Figure 4. During the measurement of a wide-range I_d from 10^{-12} to 10^{-4} A as indicated in Figure 4, V_g sweep speed depends on the current range. Therefore, an I_d - V_g hysteresis curve only gives reference information that is not suitable for accurate discussion.

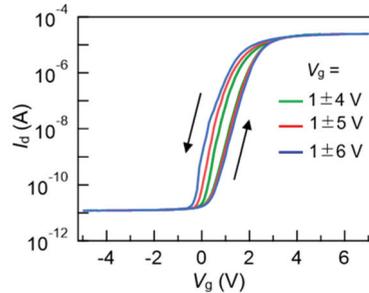


Figure 4. Static static drain current versus gate voltage (I_d - V_g) curves of a FeFET with $L_{ch} = 85$ nm. The channel width was $W = 150$ μ m. V_g ranges were $V_g = 1 \pm 4$ V, 1 ± 5 V and 1 ± 6 V.

For an accurate understanding, the FeFET performance, a pulsed V_g with a controlled time width, was applied to the FeFETs for the erase (*Ers*) or program (*Prg*) operation. The V_g pulse heights with the time widths were (V_E , t_E) for *Ers*, and (V_P , t_P) for *Prg*, respectively. For the *n*-channel-type FeFET, the V_E was negative ($V_E < 0$ V) and V_P was positive ($V_P > 0$ V) [9]. The pulse time widths t_E and t_P were the same with each other in this work ($t_E = t_P = t_{EP}$). After, *Ers* and *Prg*, I_d - V_g curves were individually measured with a small common V_g range for *Read*. Two V_{th} values were defined in the I_d - V_g curves as the V_g at $I_d/W = 1 \times 10^{-7}$ A/cm. They were expressed as V_{thE} after *Ers* and V_{thP} after *Prg*. The V_{thE} was larger than the V_{thP} [9]. The V_{th} difference of $\Delta V_{th} = V_{thE} - V_{thP}$ was defined as a memory window obtained by read operation after erase-and-program pulse applications. The memory window ΔV_{th} is normally smaller than the above-mentioned static V_w , because slow switching components in a ferroelectric do not respond to short pulses [27,72,73]. The V_{thE} and V_{thP} were investigated by repeating a series of operations: *Ers*, *Read*, *Prg*, *Read*, in this order (Figure 5a). In *Ers*, a pulsed V_g of (V_E , t_{EP}) was applied with keeping $V_d = V_s = V_{sub} = 0$ V. In *Read* after *Ers*, a V_{thE} was extracted from an I_d - V_g curve drawn by narrow-range varying V_g from 0 to 1.1 V at $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. In *Prg*, a pulsed V_g of (V_P , t_{EP}) was applied, keeping $V_d = V_s = V_{sub} = 0$ V. In *Read* after *Prg*, a V_{thP} was extracted from an I_d - V_g curve drawn under exactly the same conditions as those in *Read* after *Ers*.

Figure 5b shows V_{thE} and V_{thP} by *Read* after *Ers* and *Prg* for three sets of (V_E , t_{EP}) and (V_P , t_{EP}) of $|V_E| = V_P = 6, 7$ and 8 V. Every marker corresponds to the measured V_{thE} and V_{thP} . Memory windows, $\Delta V_{th} = V_{thE} - V_{thP}$, as a function of pulse height $|V_E| = |V_P|$ (Figure 5c) and width t_{EP} (Figure 5d) can be seen in Figure 5b, where the V_{thE} and V_{thP} results (not shown in Figure 5b) of other $V_P (= |V_E|)$ conditions were also used. Short V_g pulses of $t_{EP} = 50$ ns were available for *Ers* and *Prg* of the FeFET. Memory windows of $\Delta V_{th} > 0.7$ V were obtained using 8 and 8.5 V pulses.

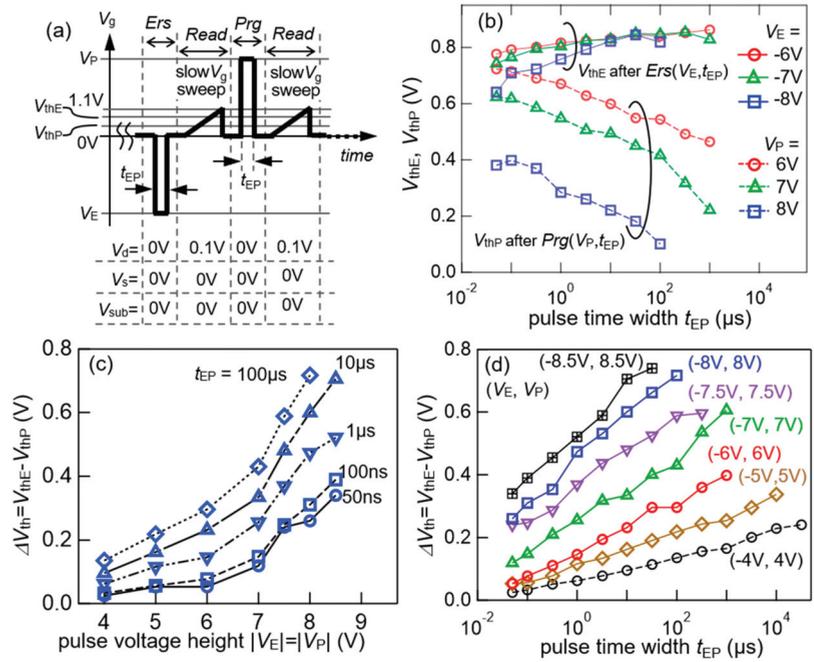


Figure 5. Investigation of V_{thE} and V_{thP} by applying V_g pulses to a FeFET with $L_{ch} = 85$ nm. The channel width was $W = 100 \mu m$. (a) The measurement procedure; (b) measured original V_{thE} and V_{thP} ; (c) pulse-height dependence of $\Delta V_{th} = V_{thE} - V_{thP}$ and (d) pulse width dependence of ΔV_{th} .

Figure 5c,d show a clear monotonic ΔV_{th} increases when raising either the pulse height or width. Good analog V_{thE} and V_{thP} controllability was suggested by smooth and linear ΔV_{th} growths with raising $\log(t_{EP})$ as shown in Figure 5d. The similar tendencies of ΔV_{th} and t_{EP} have already been reported in our previous works [3,5,7,9,52]. In the prior FeFETs, poly-crystallized ferroelectrics were visualized by electron backscatter diffraction (EBSD) [44]. The EBSD indicated that the (C)SBT consisted of multi-grains with various crystal orientations in the FeFETs. The poly-crystallized ferroelectrics may bring the analog V_{thE} and V_{thP} controllability to the FeFETs. In the present FeFET, there must be numerous grains in channel-width direction with $W = 100 \mu m$ whereas a single grain or a few were expected in channel-length with $L_{ch} = 85$ nm which was smaller than average diameters of SBT grains freely grown in-plane [44].

In a preferable geometry of the replacement-gate FeFET in the future, only the channel area $L_{ch} \times W$ will be intensively scaled down with remaining the height H . The H is decided by the gate-groove depth in *Step 7* in Section 2.1 and Figure 1. The ΔV_{th} in this report was not yet at its best ability considering the ferroelectric height $H = 450$ nm. In the vertical direction of FeFET, a gate stack by filling SBT should be essentially the same as a large L_{ch} conventional one by etching SBT. Therefore, potential ΔV_{th} will become the same as that of conventional FeFETs by improving the details in the fabrication process in Section 2.1. An immediate target for the present FeFET will be realizing $\Delta V_{th} = 0.7$ V by *Ers* of $(-6V, 10 \mu s)$ and *Prg* of $(6V, 10 \mu s)$ for $H = 190$ nm as demonstrated before using Pt/CSBT/HfO₂/Si FeFETs [7].

3.2.2. Retention

Retention of a FeFET was measured by the procedures as shown in Figure 6a,b. After program (*Prg*), *Retain* and *Read* were repeated during the scheduled time. In *Prg*, a V_g pulse of (V_P, t_{EP}) was applied with $V_d = V_s = V_{sub} = 0$ V. In *Retain*, all the terminals were kept at

zero as $V_g = V_d = V_s = V_{sub} = 0$ V. In *Read* at a certain time t , an I_d - V_g curve was drawn by varying V_g in a narrow range from 0 to 1.0 V at $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. A V_{thP} was extracted from the I_d - V_g and plotted with a marker at t as shown in Figure 6c. After completing the V_{thP} - t , V_{thE} - t started to be measured. In erase (*Ers*), a V_g pulse of (V_E, t_{EP}) was applied with $V_d = V_s = V_{sub} = 0$ V. After *Ers*, *Retain* and *Read* were repeated during the scheduled time. The *Retain* and *Read* conditions for V_{thE} - t were the same as those for V_{thP} - t . In the *Read* at a certain time t , an extracted V_{thE} was plotted with a marker at t as shown in Figure 6c. In this work, $V_P = 8$ V, $V_E = -8$ V and $t_{EP} = 10$ μ s. The retention was measured for 10^5 s in each of V_{thP} - t and V_{thE} - t . At $t = 10^5$ s, they were still distinguishable with a difference $\Delta V_{th} = 0.26$ V. When $t > 10^3$ s, as shown in Figure 6c, the gradient of the V_{thP} - $\log(t)$ and V_{thE} - $\log(t)$ curves appeared to be nearly zero. A possible ten-year retention was suggested by extrapolation lines drawn on the last three markers in both branch. The present $L_{ch} = 85$ nm FeFET showed a good retention to the same extent as those of the conventional (C)SBT FeFETs [1–9,11,12,37–40,42,45,46,52].

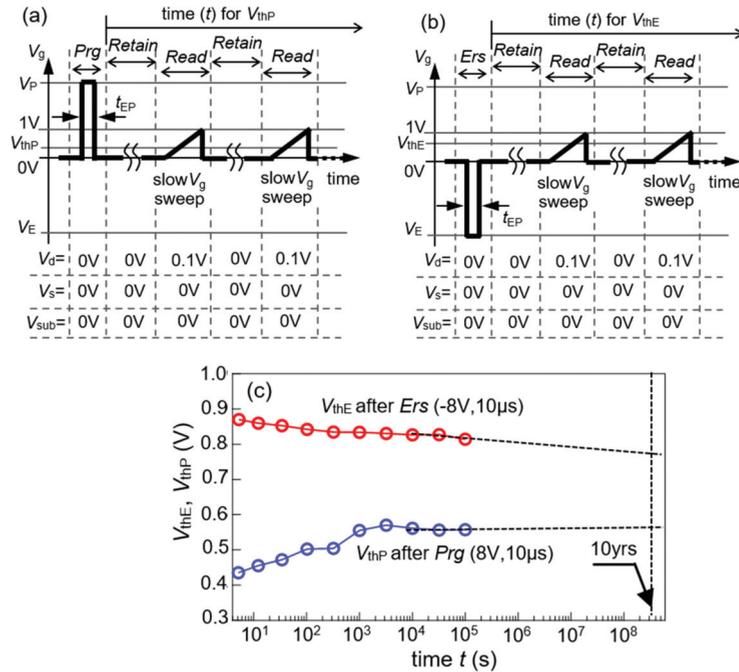


Figure 6. Retention investigation after applying V_g pulses to a FeFET with $L_{ch} = 85$ nm. The channel width was $W = 100$ μ m. The measurement procedures for the retentions of (a) V_{thP} after *Prig* of (V_P, t_{EP}) and (b) V_{thE} after *Ers* of (V_E, t_{EP}). (c) The measured retentions for 10^5 s each. Dashed lines are extrapolations of V_{thP} - $\log(t)$ and V_{thE} - $\log(t)$ for estimating V_{thP} and V_{thE} after ten years.

3.2.3. Endurance

Endurance of a FeFET was measured by the procedure shown in Figure 7a. After imposing endurance cycles on FeFETs, pairs of V_{thE} and V_{thP} were obtained. The endurance cycles consisted of periodic bipolar V_g pulses for an alternate *Ers* of (V_E, t_{EP}) and *Prig* of (V_P, t_{EP}) with $V_d = V_s = V_{sub} = 0$ V. The endurance-cycle application was interrupted at certain scheduled cycle numbers (N). After the N cycle application, V_{thE} and V_{thP} were read as follows: a series operation of *Ers*, *Read*, *Prig*, and *Read*, in this order was performed. In *Ers*, a single V_g pulse of (V_E, t_{EP}) was applied with $V_d = V_s = V_{sub} = 0$ V. In *Read* after *Ers*, an I_d - V_g was measured by varying V_g in a narrow range from 0 to 1.5 V at $V_d = 0.1$ V

and $V_s = V_{sub} = 0$ V. A V_{thE} was extracted from the I_d - V_g and plotted with a marker at N as shown in Figure 7b. In *Prg*, a single V_g pulse of (V_P , t_{EP}) was applied with $V_d = V_s = V_{sub} = 0$ V. In *Read* after *Prg*, an I_d - V_g was measured under the same conditions with *Read* after *Ers*. The obtained V_{thP} was plotted with a marker at N as shown in Figure 7b.

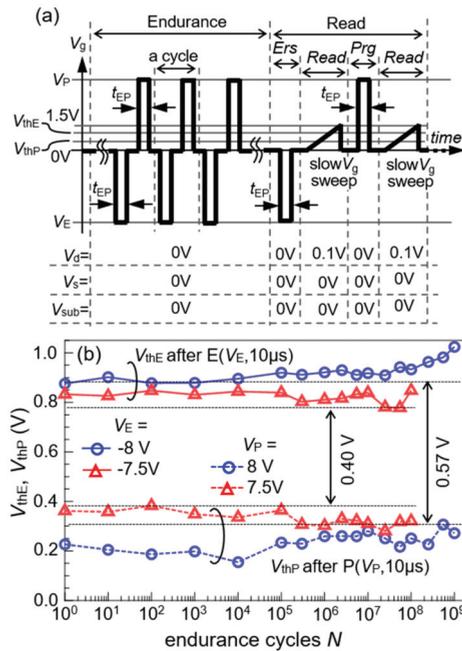


Figure 7. Endurance of a FeFET with $L_{ch} = 85$ nm. The channel width was $W = 80$ μ m. (a) The measurement procedures of applying endurance cycles and reading V_{thE} and V_{thP} . (b) Endurances were measured up to $N = 10^8$ cycles for 7.5 V V_g pulse heights and $N = 10^9$ cycles for 8 V.

As shown in Figure 7b, the *Ers* of (-7.5 V, 10 μ s) and *Prg* of (7.5 V, 10 μ s) were first applied for an endurance up to $N = 10^8$ cycles. Next, a stronger input of (-8 V, 10 μ s) and (8 V, 10 μ s) was applied to the same FeFET up to $N = 10^9$ cycles. No significant shifts of V_{thE} and V_{thP} were observed throughout the measurements. By taking the minimum of the V_{thE} and the maximum of the V_{thP} in the endurance test, $\Delta V_{th} = 0.40$ V for $|V_E| = V_P = 7.5$ V and $\Delta V_{th} = 0.57$ V for $|V_E| = V_P = 8$ V were obtained. These were margins for distinguishing V_{thE} from V_{thP} as indicated in Figure 7b. In spite of using the rather complicated dummy-gate process, the $L_{ch} = 85$ nm FeFET fabricated showed high endurance up to 10^8 – 10^9 cycles. This is the same as the endurance level that (C)SBT-FeFETs inherently have [1–12].

4. Summary

A new fabrication process of a FeFET was proposed and demonstrated. Dummy-gate patterns with self-aligned sources and drains were prepared on a Si substrate. HfO_2 with a thickness of 5 nm was inserted in advance between the dummy-gate substance and the Si substrate. The dummy substance was selectively removed to form a self-aligned groove on the gate. A thin SBT precursor film was deposited to fill up the groove. After forming the Ir gate electrode on the SBT, the whole gate stack was annealed for the SBT crystallization. The finished FeFET of Ir/SBT/ HfO_2 /Si had a channel length $L_{ch} = 85$ nm. The FeFET exhibited a 10^9 cycle-high endurance and long stable retentions measured for 10⁵ s. By adopting the replacement-gate process, area-scalable SBT-FeFETs with the high endurance and long retention were successfully produced.

Author Contributions: Conceptualization followed by numerous improvements with respect to the device structure and processing, M.T.; the anneal and MOCVD processes, S.S.; SEM observation, M.T.; creation of PC-controlled measurement programs, S.S.; electrical measurement of the devices, S.S.; data analysis and discussion, S.S. and M.T.; writing—original draft preparation, M.T.; writing—review and editing, M.T. and S.S. All authors have read and agreed to the published version of the manuscript.

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Review

On the Thermal Models for Resistive Random Access Memory Circuit Simulation

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Abstract: Resistive Random Access Memories (RRAMs) are based on resistive switching (RS) operation and exhibit a set of technological features that make them ideal candidates for applications related to non-volatile memories, neuromorphic computing and hardware cryptography. For the full industrial development of these devices different simulation tools and compact models are needed in order to allow computer-aided design, both at the device and circuit levels. Most of the different RRAM models presented so far in the literature deal with temperature effects since the physical mechanisms behind RS are thermally activated; therefore, an exhaustive description of these effects is essential. As far as we know, no revision papers on thermal models have been published yet; and that is why we deal with this issue here. Using the heat equation as the starting point, we describe the details of its numerical solution for a conventional RRAM structure and, later on, present models of different complexity to integrate thermal effects in complete compact models that account for the kinetics of the chemical reactions behind resistive switching and the current calculation. In particular, we have accounted for different conductive filament geometries, operation regimes, filament lateral heat losses, the use of several temperatures to characterize each conductive filament, among other issues. A 3D numerical solution of the heat equation within a complete RRAM simulator was also taken into account. A general memristor model is also formulated accounting for temperature as one of the state variables to describe electron device operation. In addition, to widen the view from different perspectives, we deal with a thermal model contextualized within the quantum point contact formalism. In this manner, the temperature can be accounted for the description of quantum effects in the RRAM charge transport mechanisms. Finally, the thermometry of conducting filaments and the corresponding models considering different dielectric materials are tackled in depth.

Keywords: resistive memories; thermal model; heat equation; thermal conductivity; circuit simulation; compact modeling; resistive switching; nanodevices

1. Introduction

Resistive memories (also known as resistive random access memories or RRAMs) base their operation on resistive switching mechanisms to modulate their conductance in a non-volatile manner [1–3]. Their promising potential is subject to scrutiny both in academia and in industry. These devices could be alternatives to flash devices in applications related to their non-volatility, such as storage class memories [4]. RRAMs show short read/write times, good enough endurance and retention behavior, low power operation, CMOS technology compatibility and the possibility to be built on 3D stacks [1,2]. Apart from non-volatile memory circuits, where certain applications are currently on the market, RRAMs show great potential for cryptographic circuits due to their inherent stochasticity, which can be employed for the design of random number generators and physical unclonable functions [5–9]. Nevertheless, currently, the hottest application for these devices is linked to neuromorphic circuits [10–15]. RRAMs can mimic biological synapses within a fully compatible CMOS technology context to facilitate the fabrication of hardware neural networks. This approach allows the use of a lower number of electronic components (by means of RS device crossbars) and low power consumption [1,10,11,14,16] than the purely CMOS alternative to neuromorphic circuits firstly introduced by Mead in the late eighties [17]. The number of papers on this subject including resistive switching devices is growing by leaps and bounds. Nevertheless, different issues should be improved for these devices in order to overcome the difficulties connected to massive industrial use; among them, the following should be counted: great temperature sensitivity, manufacturing processes, variability and the lack of well-established electronic design automation (EDA) tools, including in the latter issue strategies for parameter extraction. In relation to these essential aspects, we will deal here with the device thermal description and its modeling from a circuit simulation perspective.

The development of RRAM simulation and modeling infrastructure is key to step forward into industrial mature applications. In this respect, in the memory realm, it is important to highlight that DRAM and NAND Flash technologies will continue to hold their ground and even advance despite the slowing of Moore's Law in the short-medium term. Although a great number of papers have been published so far on modeling and simulation issues [18–41], there are many open questions that need to be addressed to improve RRAM position in the EDA context. One of the pressing modeling questions is connected with the device inherent stochasticity that produces cycle-to-cycle variability [19,42–51]. This type of variability has to be managed to achieve RRAM technological maturity; however, even if a variability reduction is achieved, taking into consideration its nature in the modeling is a must [52]. Another modeling battlefield lies in what is linked to thermal effects. It is known that most RS mechanisms are thermally activated [19,23,32,53–57]. The temperature evolution produced by Joule heating in device-relevant regions, where charge conduction is concentrated, determines the operation in many different types of RRAMs [18,19,38,53,58–60]. Consequently, an accurate thermal description is essential to implement both good RRAM physical simulators and compact models. It is also important to highlight that in cross-bar architectures, an optimum topology for hardware neural network implementation among other applications, the thermal evolution of one device might be influenced by neighbor cells. This effect, known as thermal crosstalk [60–63], has to be considered at the integration stage of chips based on RS devices.

Modeling of RRAM, as well as its physical simulation in general, shows notorious differences with respect to other electron devices. In this respect, in devices such as MOSFETs [64,65] (even multigate FETs [66]) or diodes [67,68], once a reasonable grid is established, the main differential equations are discretized and, in general, but for very scarce cases, convergence is searched for to obtain a solution. This is the main scheme to follow in drift-diffusion, hydrodynamic and Monte Carlo simulation approaches [69]. By contrast, in RRAMs the modeling paradigm is different due to the particularities of their operation. For the initial forming process (a pristine dielectric is assumed) and further set processes within RS cycles (in the common filamentary conduction regime, the case

we will deal with henceforth), a conductive filament (CF) through the dielectric is formed which shorts the device electrodes and greatly reduce the device resistance [2,70]. Non-linear physical mechanisms (mostly thermally activated, following an Arrhenius' equation relationship) come into play in a positive feedback loop that leads certain magnitudes, such as the temperature, to shoot up. This process has an obvious reflection at the experimental level, the current has to be limited to avoid the device hard breakdown and its consequent destruction. All this leads to the caveat that we have to deal with numerical divergence from the simulation viewpoint. The current is limited in the context of forming or set processes to avoid the device rupture; in this manner, an uncontrolled temperature rise and the corresponding CF quick growth is avoided because after a hard breakdown process RS operation does not hold. At the simulation level, a current limit is also needed. The reset process is also linked to RRAM simulation divergence. As the reset goes on, the CF shrinks and the same current is strangled in a CF narrow section. Hence, Joule heating produces a temperature increase at this CF narrowing. The thermally activated mechanisms in the CF narrowing surroundings rise exponentially and the CF rupture takes place. If the rupture is thermally controlled, as in many unipolar devices, it is based upon a thermal run-away process that leads to the CF destruction. In summary, for a correct RRAM simulation description (both at the device and circuit levels, in the latter case it would be a compact modeling approach), we have to face numerical divergence in addition to nonlinearity in some of the physical magnitudes at hand in one way or other. This means, in general, as the reader can imagine, a numerical nightmare. For instance, when you set up a limit for the compliance current, there might be an important difference between the iteration prior to achieving the current limit and the following step (once the compliance current has been exceeded) in terms of the CF size and temperature in the hottest spot. If you miss to stop the iterations just when the compliance current is reached, and for some reason you iterate once more within the positive feedback loop the device is going through, you can end up wondering what is the dielectric melting temperature.

There are different RRAM models in the literature, and most of them consider thermal effects in one way or another. Some assume a simplified version of the steady-state heat equation (HE); others account for a non-steady-state model where the heat capacitance is included. In general, the main differences are found in the boundary conditions formulation to describe the device physics in the context of the HE or an equivalent energy balance equation. In any case, all these models can be formulated using the standard description proposed by [71], where they fit naturally. By using this formulation, it is clear that all these devices can be considered as extended memristors, this being the most general class of memristor devices according to usual classification [72]. Notice that, from this point of view, RRAM devices can be used inside the memristor framework as circuital elements for purposes further than memory applications [73–75].

Different flavors of these thermal models have been reported; however, as far as we know, they have not been brought together under one roof yet as has been done, for example, with electrical models [41]. We do so here. In Section 2, we comment on the HE in the RRAM operation context, in particular, we explain 3D physical simulation and compact modeling focusing on thermal effects. Section 3 is devoted to the RRAM thermal description through a general memristor model; the RRAM quantum point contact modeling including thermal effects is unfolded in Section 4, and finally, the thermometry of conducting filaments and corresponding modeling is developed in Section 5.

2. Mathematical Description of RRAM Thermal Effects

2.1. Heat Equation

We start by taking the 3D heat equation in the device into consideration, Equation (1):

$$\nabla \cdot (k_{th}(\mathbf{r}) \nabla T(\mathbf{r}, t)) + \dot{e}_{generated}(\mathbf{r}) = \rho(\mathbf{r})c(\mathbf{r}) \frac{\partial T(\mathbf{r}, t)}{\partial t} \quad (1)$$

where k_{th} —stands for the thermal conductivity (W/(m K)). This parameter depends on the temperature and geometry (assuming different material layers, which is the case for the usual RRAM architecture), c —stands for the specific heat or specific heat capacity (J/(kg K)). It is assumed that we are considering the specific heat capacity at constant pressure, which is why it is also denoted as c_p , ρ —stands for the material density (kg/m³) and $\dot{e}_{generated}$ —stands for the power density generated (rate of heat generation by means of Joule heating, per unit volume inside the system we are considering). It can be calculated as $\sigma(r)E^2(r)$, where $\sigma(r)$ is the local electrical conductivity and $E(r)$ is the local electric field [18,38]; i.e., the product of the field and the current density.

The RRAM thermal description requires the solution of this equation in the whole device active region. Nevertheless, in the compact modeling approach (CMA) some simplifying assumptions are made. Among others, we consider this equation in the region close to the conductive filament, where charge conduction takes place after a successful set or forming process (when the CF is created the device is said to be in the low resistance state, LRS, while if the CF is ruptured, after a successful reset process, the device resistance is much higher, the device enters in the high resistance state, HRS). If all the different device material layers are included (dielectric, possibly a multilayer stack, electrodes, etc.), the thermal conductivity, the density and specific heat of the different materials have to be considered [29,76,77].

A step forward consists in using the 1D HE version (a simplifying assumption that works well in many cases). If the x coordinate is assumed to be parallel to the CF longitudinal axis, from one of the dielectric-electrode interfaces to the other, and the CF is considered to be narrow enough to consider the same temperature in the transverse sections perpendicular to the x -axis; then, the HE could be written as follows:

$$\frac{\partial}{\partial x} \left(k_{th}(x) \frac{\partial T(x, t)}{\partial x} \right) + \dot{e}_{generated}(x) = \rho(x)c(x) \frac{\partial T(x, t)}{\partial t} \quad (2)$$

This equation is most of the times solved within the device conductive filament, whose geometry is assumed to be a cylinder or a truncated-cone. For the HE particularization in the RRAM CMA some further assumptions are employed for the sake of simplicity:

- (a) Constant thermal conductivity, i.e., $k_{th}(x, T) = k_{th}$. Neither geometric nor temperature dependencies are considered. In most cases, the CF thermal conductivity is the one considered.
- (b) A single temperature in the whole conductive filament [38,78] is taken into account (this means a strong simplifying approach). Some models for circuit simulation can account for two different temperatures [79], this is a good strategy since the key (higher) temperature at the CF narrowing, where the CF is ruptured, is decoupled from the main CF bulk temperature; this latter temperature does not increase in the same manner. See Figure 4c in [80], where the CF temperature along the dielectric is plotted for different voltages. It is clear that the temperature is much higher in the CF narrowing while it shows a different behavior for the main CF body. The model with two different CF temperatures is more complex, hence, this issue has to be taken into account when dealing with circuits including hundreds or thousands of components.

Different RRAM cell schematics are shown in Figure 1. Assuming filamentary conduction, the CF evolution has to be calculated to describe RS operation and determine the device current. Several CF types (shapes) from the CMA employed in the literature are represented in Figure 1.

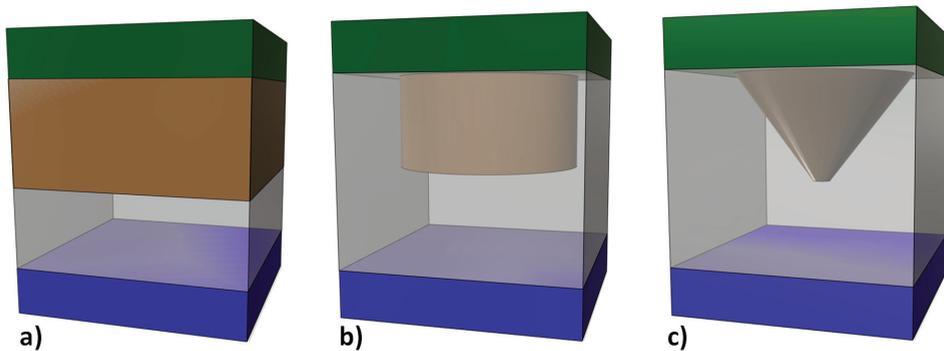


Figure 1. Different conductive filament shapes employed in RRAM compact models for circuit simulation. We will use this CF shapes in the thermal models described below. (a) CF that occupies all the modeling domain, (b) cylindrical CF, (c) truncated-cone shaped CF.

2.2. A Numerical Approach for the Heat Equation

Equation (1) is essential to all types of RRAM physical simulators. It is usually auto-consistently solved with other differential equations (Poisson equation, kinetic equations for the chemical reactions that control the CF evolution, etc.) [21,23,34,53,70,77,81]. Since the most common device structure is not based on curved surfaces or volumes, even in the more scaled cases, a finite difference approach could be a reasonable choice that simplifies the grid and the differential equations discretization. Boundary conditions are key to describe correctly the physics of the device operation. In many simplified models, the electrodes are supposed to be perfect heat sinks and, therefore, Dirichlet's boundary conditions are established at the electrode-dielectric interface (in most cases room temperature is assumed at this interface). However, to correctly describe heat transfer between the conductive filament, the dielectric layer and the electrodes, some parts of the latter should be included in the simulation domain (SD). The SD lateral interfaces (perpendicular to the dielectric-electrode interface) are usually described by Neumann boundary conditions. Sometimes the temperature derivative in the normal direction of these interfaces is assumed to be null. This means adiabatic conditions accordingly with Fourier's law for heat conduction.

We have included here some results to illustrate the HE role in a RRAM simulator. Our simulator calculates the RRAM current in the LRS. The internal resistance calculation is performed assuming fully formed metallic-like conductive filaments of different shapes. In addition to the current calculation, we solve the 3D HE [29]. In the SD we have included the dielectric stack and part of the electrodes; precisely, 10 nm of the Si-n⁺ (bottom electrode) and Ni (top electrode). Consequently, the SD thermal boundary is shifted from the dielectric/electrode interfaces to the electrodes, as commented above. A 40 nm (X axis) × 40 nm (Y axis) × 30 nm (Z axis, vertical axis running from the Si layer to the Ni layer) SD is considered, see Figure 2.

Dirichlet's boundary conditions were supposed at the outer electrode layer surfaces. The constant temperature located outside the device was room temperature (a reasonable assumption accounting for the high electrode thermal conductivity). For the SD lateral faces we employed perfectly matched layers (PML) [82], an improved implementation of Neumann boundary conditions since PML are particularly appropriate for differential equation solution to deal with open boundary problems, our case here [83]. Joule heating takes place in the CFs. Some devices (schematics shown in Figure 2) were simulated. In our simulations we included two CFs to account for a different device configuration with respect to conventional studies with just one CF.

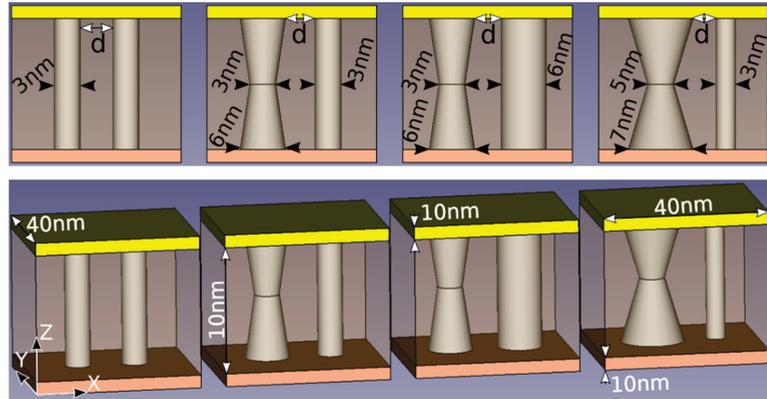


Figure 2. Simulated RRAMs. Four different LRS situations are considered, in all cases a double conductive filament was employed assuming a distance, d , between them (the bottom and top figures are the same in each case from different perspectives). The bottom electrode is assumed to be Si- n^+ and the top electrode is made of Ni, the dielectric consists of HfO_2 . The conductive filament shapes employed are shown for the different cases under study, they are assumed to be metallic-like, formed by Ni atom clusters [24,55,80]. The physical parameters are the same employed in the simulation in [29].

In Figure 3, symmetric temperature distributions are observed in (a) and (b), corresponding to similar CFs, and therefore, to alike Joule heating effects. See the effects of the low thermal conductivity in the dielectric. According to Fourier’s law for heat conduction, the heat flux, q , is equal to the product of thermal conductivity, k_{th} , and the negative local temperature gradient ($q = -k_{th}\nabla T$). Since the HfO_2 thermal conductivity is around $1\text{ W}/(\text{K m})$, the temperature drops off rapidly around the CF. See also the effects of the dielectric-electrode boundary at $z = 10\text{ nm}$ and $z = 30\text{ nm}$, the temperature reduction is different from what is seen in the CF perpendicular direction along the x -axis. The maximum temperature is obtained in the narrowest section for the symmetrical truncated-cone shaped CF, as seen in (c) and (d). At this point, the physical mechanisms behind RS are more active and, consequently, they trigger the CF rupture at this location. See the thermal connection between the CFs for the different shapes and distances in between; in this respect, in tree-branch shaped filaments, the destruction of the branches and the thermal and current redistribution in the remaining intertwined branches makes the reset a complicated process.

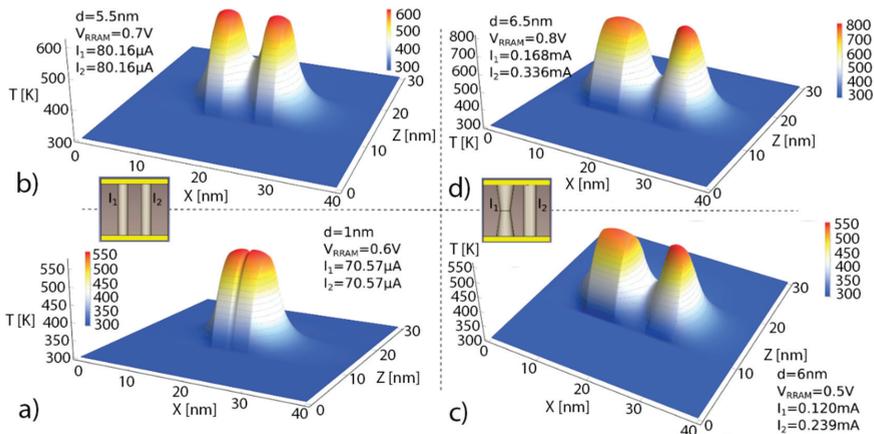


Figure 3. Temperature plots for some of the devices simulated as explained above (see the insets), the cross-section cuts corresponds to $y = 20\text{ nm}$ in our SD. (a) RRAM with two cylindrical CFs (diameter = 3 nm) separated 1 nm apart for a bias of 0.6 V .

(b) RRAM with two cylindrical CFs (diameter = 3 nm) separated 5.5 nm apart for a bias of 0.7 V. (c) RRAM with one cylindrical CF (diameter = 6 nm) and a symmetrical truncated-cone shaped CF (low diameter = 3 nm, high diameter = 6 nm) separated 6 nm apart for a bias of 0.5 V. (d) RRAM with one cylindrical CF (diameter = 6 nm) and a symmetrical truncated-cone shaped CF (low diameter = 3 nm, high diameter = 6 nm) separated 6.5 nm apart for a bias of 0.8 V. For the sake of visibility, some of the 3D plots are rotated with respect to the 2D CF scheme.

In Figure 4 simulations of other RRAM configurations are shown. See that small changes in the device voltage can lead to important temperature variations in the CF bottleneck where RS mechanisms are thermally enhanced. In (c) and (d), the thermal cross-talk between CFs is observed when the distance between CFs is around 1 nm. For much higher inter CF distances, a lower thermal connection results even for higher currents.

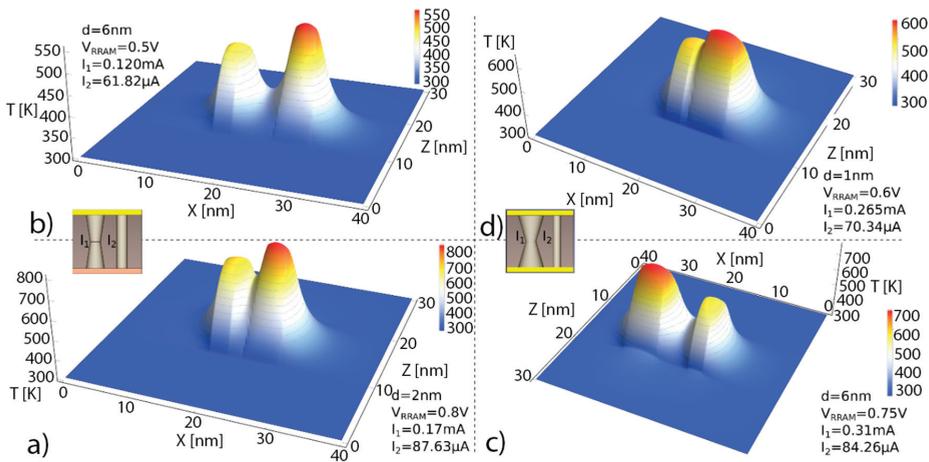


Figure 4. Temperature plots for some of the devices simulated as explained above (see the insets), the cross-section cuts corresponds to $y = 20$ nm in our SD. (a) RRAM with one cylindrical CF (diameter = 3 nm) and a symmetrical truncated-cone shaped CF (low diameter = 3 nm, high diameter = 6 nm) separated 2 nm apart for a bias of 0.8 V. (b) RRAM with one cylindrical CF (diameter = 3 nm) and a symmetrical truncated-cone shaped CF (low diameter = 3 nm, high diameter = 6 nm) separated 6 nm apart for a bias of 0.5 V. (c) RRAM with one cylindrical CF (diameter = 3 nm) and a symmetrical truncated-cone shaped CF (low diameter = 5 nm, high diameter = 7 nm) separated 6 nm apart for a bias of 0.75 V. (d) RRAM with one cylindrical CF (diameter = 3 nm) and a symmetrical truncated-cone shaped CF (low diameter = 5 nm, high diameter = 7 nm) separated 1 nm apart for a bias of 0.6 V. For the sake of visibility, some of the 3D plots are rotated with respect to the 2D CF scheme.

2.3. Explicit Heat Equation Solutions

2.3.1. RRAM with a Cylindrical Filament (Steady-State Operation, No Heat Transfer Term)

In the case under consideration, we assume a cylindrical CF with constant electrical and thermal conductivities. The boundary conditions are established at the extremes of the filament ($x = 0$ and $x = t_{ox}$, respectively, with temperatures $T(x = 0) = T(x = t_{ox}) = T_0$, where t_{ox} stands for the dielectric thickness), see Figure 5.

From Equation (2), we obtain [38]:

$$\sigma E^2 = -k_{th} \frac{\partial^2 T(x)}{\partial x^2} \tag{3}$$

where E is the constant electric field in the CF ($E = V_{RRAM}/t_{ox}$). Figure 5 shows the different elements taken into account to solve the HE. The solution for the maximum temperature in the middle of the CF, with the boundary conditions sketched in Figure 5, is:

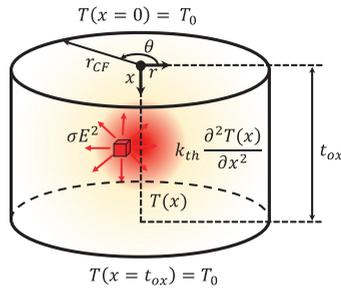


Figure 5. Schematic showing the different elements considered to solve the simplified HE in a cylindrical and homogenous conductive filament.

$$T_{max} = T_0 + \frac{\sigma t_{ox}^2 E^2}{8 k_{th}} \tag{4}$$

The single temperature that will represent the whole CF thermal state is chosen to be T_{max} , as shown below (see Appendix D.3 in [84]),

$$T_{max} = T_0 + \frac{\sigma V_{RRAM}^2}{8 k_{th}} \tag{5}$$

Henceforth, this will be our thermal model 1, TM1. This assumption is justified by the fact that this maximum value controls the physical mechanisms that lead to the CF narrowing in a reset process and finally to the CF rupture. Nevertheless, among other issues in this model, the calculation of the ohmic resistance as the CF heats up is not correctly solved since the main CF body remains at a temperature much lower than the hottest spot where the maximum temperature is achieved. The Verilog-A implementation is shown in Table 1 (TM1).

2.3.2. RRAM with a Cylindrical Filament Including a Heat Transfer Term (Steady-State Operation)

We have added a term to account for the heat transfer from the CF to the surrounding insulator to Equation (3), see Figure 6. The heat losses are included by means of the heat transfer coefficient (h) [31,38,79,85], see Equation (6):

$$\sigma E^2 = -k_{th} \frac{\partial^2 T(x)}{\partial x^2} + 2 h \frac{T(x) - T_0}{r_{CF}} \tag{6}$$

where r_{CF} stands for the conductive filament radius.

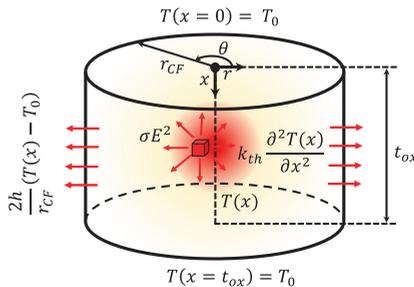


Figure 6. Sketch of a cylindrical filament with the different terms in the HE shown in Equation (6), including the heat transfer term.

Table 1. Verilog-A implementation of some of the thermal models described.

Thermal Model	Verilog-A Code for the Temperatures Calculation
TM1	$T = T_0 + \sigma V^2 / (8.0 \cdot kth);$
TM2	$E = V / tox;$ $\alpha = tox / 2.0 \cdot \sqrt{2 \cdot h / (kth \cdot rcf)};$ $T = T_0 + (\sigma E^2 \cdot rcf \cdot (\exp(\alpha) - 1)^2) / (2 \cdot h \cdot (\exp(2 \cdot \alpha) + 1));$
TM3	$LCF = tox - g;$ $rg = \sqrt{rt \cdot rb};$ $\eta = rt / rb;$ $E = V / LCF;$ $\alpha = LCF \cdot \sqrt{2 \cdot h / (kth \cdot rg)};$ $T = T_0 + rg \cdot \sigma E^2 / (\eta \cdot h) \cdot (0.5 - (\exp(\alpha / 2.0) / (\exp(\alpha) + 1)));$ analog function real fdt ₀ ; real sigmat,rcf,E,alpha; input sigmat,rcf,E,alpha; begin fdt ₀ = sigmat*rcf*E**2*tanh(alpha*tox/2.0)/(sqrt(2*kth*h*rcf)); end endfunction analog function real fT; real sigmat,rcf,eta,alpha,dt ₀ ; input sigmat,rcf,eta,alpha,dt ₀ ; begin fT = T ₀ + sigmat*rcf*E**2/(2*h)*(1-cosh(alpha*tox/2.0)) + dt ₀ /alpha*sinh(alpha*tox/2.0); end endfunction analog function real falpha; real rcf; input rcf; begin falpha = sqrt(2*h/(kth*rcf)); end endfunction analog function real fsigmat; real T; input T; begin fsigmat = sigma/(1 + alphas * (T - T ₀)); end endfunction
TM4	

Equation (6) can be solved and the result is given below [27],

$$T_{max} = T_0 + \frac{\sigma E^2 r_{CF} (e^\alpha - 1)^2}{2 h (e^{2\alpha} + 1)} \quad (7)$$

where:

$$\alpha = \frac{t_{ox}}{2} \sqrt{\frac{2 h}{k_{th} r_{CF}}} \quad (8)$$

In this case, as before, the electric field is assumed constant, and the CF temperature is considered to be T_{max} , as calculated in Equation (7). We will consider this the thermal model 2, TM2 (see the Verilog-A code in Table 1).

2.3.3. RRAM with a Truncated-Cone Shaped Filament Including Heat Transfer Coefficient (Steady-State Operation)

The boundary conditions and the CF geometry for this model are shown in Figure 7. Notice that the CF radius $r_{CF}(x)$ of the truncated cone depends on the x position. Consequently, the heat equation can be expressed now as follows:

$$\sigma(x) E(x)^2 - \frac{2h}{r_{CF}(x)} (T(x) - T_0) = -k_{th} \frac{\partial^2 T(x)}{\partial x^2} \tag{9}$$

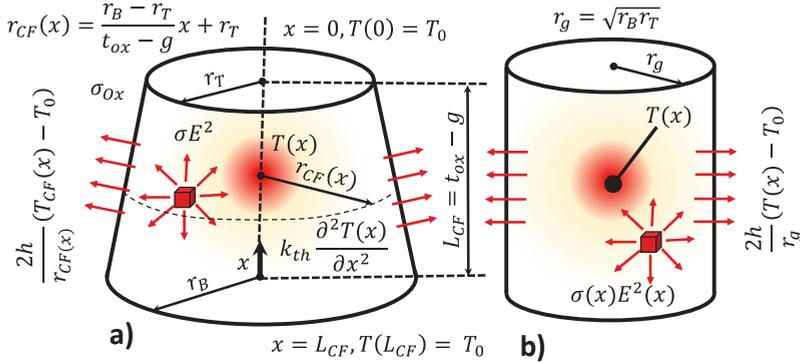


Figure 7. (a) Energy dissipation terms included in the heat equation and geometrical domain for the CF thermal description, (b) cylindrical CF equivalent employed to simplify the HE solution and obtain a compact analytical expression for the CF temperature. Note that the conductive filament length (L_{CF}) can be lower than the oxide layer (t_{ox}), due to the gap (g) between the top electrode and the conductive filament tip (see [27,78,86–88]).

This equation cannot be solved analytically because of the variable CF radius, $r_{CF}(x)$. In order to obtain an approximated analytical solution, we considered a transformation to simplify. A truncated-cone shaped CF with constant conductivity was found to be approximately equivalent in terms of this calculation to a cylinder with radius ($r_g = \sqrt{r_T r_B}$) and variable conductivity $\sigma_{CF}(x)$ [27], see Figure 7. For a fixed applied voltage, we include the maximum electric field. This value is affected by the ratio between the two truncated-cone radii ($\eta = r_T/r_B$). Under this assumption, the following simplified HE was obtained:

$$\frac{\sigma V_{RRAM}^2}{L_{CF}^2 \eta} - \frac{2h}{r_g} (T(x) - T_0) = -k_{th} \frac{\partial^2 T(x)}{\partial x^2} \tag{10}$$

Using this parameter:

$$\alpha = L_{CF} \sqrt{\frac{2h}{k_{th} r_g}} \tag{11}$$

The value of T_{max} can be obtained as follows (the one we assume for the whole CF, this will be the thermal model 3, TM3, see the Verilog-A code in Table 1),

$$T_{max} = T_0 + \frac{r_g \sigma E^2}{\eta h} \left[\frac{1}{2} - \frac{e^{\frac{\alpha}{2}}}{e^{\alpha} + 1} \right] \tag{12}$$

2.3.4. RRAM with a Truncated-Cone Shaped Filament Including Heat Transfer Coefficient (Steady-State Operation) and Two Temperature Values to Represent the CF Thermal Behavior

The use of two different CF temperatures allows a more accurate thermal description of the CF narrowing, where the temperature rises due to the thermal run-away process that leads to the RS operation, and a CF bulk temperature that accounts for the temperature in

the CF wider part. This CF region could be left almost untouched in the sequence of set and reset processes. We will consider this version the thermal model 4, TM4 (see in Table 1 a Verilog-A implementation of the first thermal models proposed here). In the approach we followed, the electric field is calculated by means of two components associated with the CF top and bottom parts [79]. In this respect, the electric field can be calculated as: $E_{(T,B)} = \frac{V_{(T,B)}}{L/2}$, where $V_{(T,B)}$ is obtained considering the voltage divider formed by the resistances associated with the CF top and bottom portions (see the Appendix in [79]).

In the approximation strategy developed here, the maximum temperature (see the previous thermal models) is obtained for two cylinders of different radii (associated to the top and bottom CF temperatures), see Figure 8. These values are assumed to be the temperatures at the main CF volumes linked to the cylinders: for the thicker CF section (Figure 8b), T_T , and for the narrow CF (Figure 8c), T_B . The analytical expression for the temperature calculation is given below:

$$T_{(T,B)} = T_0 + \frac{\sigma_{(T,B)} r_{CF(T,B)} E_{(T,B)}^2}{2h} \left(1 - \cosh\left(\frac{\alpha_{(T,B)} t_{ox}}{2}\right) \right) + \frac{dT_{0(T,B)}}{\alpha_{(T,B)}} \sinh\left(\frac{\alpha_{(T,B)} t_{ox}}{2}\right) \quad (13)$$

where, parameters $\alpha_{(T,B)}$ and $dT_{0(T,B)}$ are given in the equations below [79]:

$$\alpha_{(T,B)} = \sqrt{\frac{2h}{k_{th} r_{CF(T,B)}}} \quad (14)$$

$$dT_{0(T,B)} = \frac{\sigma_{(T,B)} r_{CF(T,B)} E_{(T,B)}^2 \tanh\left(\frac{\alpha_{(T,B)} t_{ox}}{2}\right)}{\sqrt{2k_{th} h r_{CF(T,B)}}} \quad (15)$$

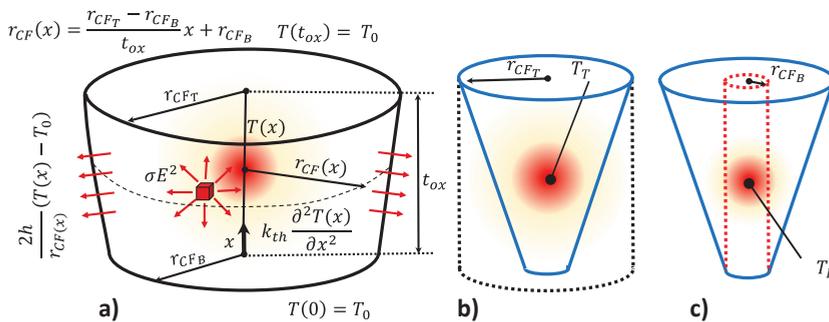


Figure 8. RRAM cell CF scheme for the thermal model based on two different CF temperatures. (a) Original filament with the corresponding boundary conditions. Cylindrical CFs (shown in dashed lines) employed to compute the (b) top temperature T_T and (c) the bottom T_B .

Equation (16) includes the CF conductance temperature dependence, assuming a metallic behavior:

$$\sigma_{(T,B)} = \frac{\sigma_0}{1 + \alpha_T (T_{(T,B)} - T_0)} \quad (16)$$

where σ_0 stands for the CF conductivity at room temperature (T_0) and α_T is the conductivity temperature coefficient. The Verilog-A code is shown in Table 1 (TM4).

2.4. Energy Balance in the Device

If we apply the first law of thermodynamics in terms of an energy balance in the device active region, we would obtain Equation (17) [78]:

$$\dot{e}_{generated} - \kappa(T(t) - T_0) = C_{th} \frac{\partial T(t)}{\partial t} \tag{17}$$

where T_0 stands for the temperature of the dielectric that surrounds the CF (usually assumed at room temperature) and κ is the inverse of the thermal resistance. In this case we do not account for a temperature distribution along the CF as in Equation (2). Our perspective here accounts for the whole CF, and even its surroundings, which is represented by a single temperature. In addition, we do not follow, as above, a scheme based on the HE solution and the association of the maximum temperature with the CF. The power generated can be calculated as $V_{RRAM}(t)I_{RRAM}(t)$, although we will employ $V(t)I(t)$ for short. We can study this differential equation accounting for different operation regimes.

2.4.1. Steady-State

This regime works well under the conventional ramped voltage stress, RVS. With long ramps to switch the device, Equation (17) can be written as follows:

$$\dot{e}_{generated} = \kappa(T(t) - T_0) \tag{18}$$

The power generated in the conductive filament (CF) (Joule heating effects calculated as current x voltage) equals the power dissipated toward the electrodes and the dielectric. Under the consideration of a single temperature to characterize the device active region, assuming that the electrodes and the dielectric are perfect heat sinks at a fixed temperature, T_0 , Equation (18) can be written as follows:

$$R_{th} = \frac{T - T_0}{VI} \tag{19}$$

where R_{th} stands for the effective thermal resistance (it depends on the device physical features and is associated with heat conduction [89]). Using this simple model (thermal model 5, TM5), the device temperature can be estimated from Equation (19) [88,90–94].

At circuit simulation level, Equation (19) can be implemented with the equivalent electrical sub-circuit shown in Figure 9. The heat dissipated power is represented by a dependent current source whose value is described as $G_1 = VI$, where the voltage is determined by the two input sub-circuit terminals V^+ and V^- , and the current is sensed by a null voltage source V_{sense} connected in series between the input terminals I^+ and I^- . The thermal resistance is represented by an electrical resistance, R_{th} , and the room temperature by a constant voltage source, T_0 , with a value that equals the room temperature (T_0), in K. The output sub-circuit terminal (T) provides a voltage that represents the device temperature T (in K).

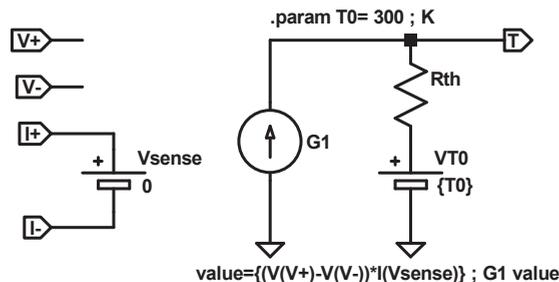


Figure 9. Equivalent electric circuit for the RS device thermal model based on a thermal resistance R_{th} .

2.4.2. Non-Steady-State Approach

Models based only on thermal resistances do not provide capacitive effects in terms of transient operation (mostly related to pulsed voltage stress, PVS, that can be employed to tune the device resistance in a multilevel operation regime, as needed in neuromorphic circuits). In order to include thermal inertia in the model, a capacitor (in the electrically equivalent thermal circuit) is added, C_{th} , the thermal or heat capacitance. This approach is used in different RRAMs compact models (thermal model 6, TM6), [78,95,96]. We can reformulate Equation (17) to the following expression:

$$VI = \frac{T - T_0}{R_{th}} + C_{th} \frac{dT}{dt} \quad (20)$$

From Equation (20), the temperature can be obtained as:

$$T = T_0 + VI R_{th} - \tau_{th} \frac{dT}{dt} \quad (21)$$

where τ_{th} (thermal time constant) is defined as follows:

$$\tau_{th} = C_{th} R_{th} \quad (22)$$

Equation (20) can be solved analytically if we assume a constant voltage (see Equation (23)).

$$T(t) = T_0 + VI R_{th} \left(1 - e^{-\frac{t}{\tau_{th}}}\right) \quad (23)$$

If we apply a time-dependent voltage, $V(t)$, Equation (23) does not work. In this case, we have to solve numerically Equation (20). Assuming a new function, $X(t) = T(t) - T_0$, we obtain,

$$V(t)I(t) = \frac{X(t)}{R_{th}} + C_{th} \frac{dX(t)}{dt} \quad (24)$$

Discretizing under equally distant temporal points $t_{i+1} = t_i + \Delta t$:

$$V_i I_i = \frac{X_i}{R_{th}} + C_{th} \frac{X_{i+1} - X_i}{\Delta t} \quad (25)$$

which gives us:

$$R_{th} V_i I_i = X_i + \tau_{th} \frac{X_{i+1} - X_i}{\Delta t} \quad (26)$$

and consequently,

$$X_{i+1} = \frac{\Delta t}{\tau_{th}} (R_{th} V_i I_i - X_i) + X_i \quad (27)$$

Finally, the device temperature could be calculated as $T_{i+1} = X_{i+1} + T_0$. From a circuit simulation point of view, Equation (20) can be implemented with the equivalent electrical sub-circuit shown in Figure 10. The values of the different electric elements and the role of the pins is the same as in Figure 9. However, a capacitor has been added to account for the thermal capacitance.

The values $\kappa = 2.8\text{--}25 \mu\text{J}/\text{K s}$ ($R_{th} = 4 \times 10^4\text{--}3.5 \times 10^5 \text{ K/W}$) and $C_{th} = 0.04\text{--}1.1 \text{ pJ}/\text{K}$ were employed in [78]. In [95], the following values were given: $C_{th} = 0.318 \text{ fJ}/\text{K}$ and $\tau_{th} = 0.23 \text{ ns}$, from them the thermal resistance can be extracted $R_{th} = \tau_{th}/C_{th} = 7.23 \times 10^5 \text{ K/W}$. The thermal resistance in [91] was taken $R_{th} = 5 \times 10^5 \text{ K/W}$. An estimation of 33 ps for the thermal time constant is reported in [18], which has to be compared to the electric pulse-width to assess the importance of thermal transient effects in conventional RRAM operation. The heat capacitance can be calculated as $C_{th} = C_p t_{ox} A$ [18], where A is the CF effective area, the effective CF length that approximately corresponds to the dielectric thickness (t_{ox}) and

C_p is the volumetric heat capacity (calculated as $\rho \times c$, Equation (2)) [89]. As detailed in [18], the thermal resistance can be calculated as follows:

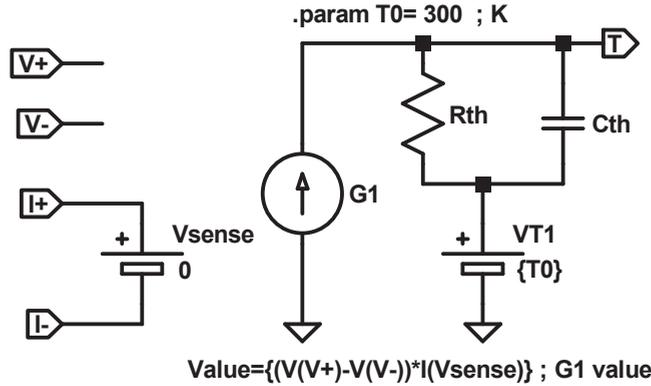


Figure 10. Equivalent electric circuit of a RRAM thermal model based on a thermal resistance and capacitance to implement Equation (20).

$$R_{th} \approx \frac{t_{ox}}{k_{th} A} \tag{28}$$

Assuming as the reference material Hf, we have the following values $k_{th} = 23 \text{ Wm}^{-1}\text{K}^{-1}$, and $C_p = 1.92 \text{ JK}^{-1}\text{cm}^{-3}$. Therefore, the thermal time constant can be estimated as:

$$R_{th}C_{th} = \frac{C_p t_{ox}^2}{k_{th}} \tag{29}$$

which is 33 ps for the case considered ($t_{ox} = 20 \text{ nm}$).

A quick estimation to assess the role of the thermal resistance ($R_{th} = 4 \times 10^4 \text{ K/W}$) can be performed if we assume an ideal device in the LRS under a steady-state regime with $I_{RRAM} = 1 \text{ mA}$ and $V_{RRAM} = 1 \text{ V}$; using Equation (19), we would have $T = T_0 + R_{th} \times I \times V = T_0 + 40 \text{ K}$, or $T = T_0 + 500 \text{ K}$, if $R_{th} = 5 \times 10^5 \text{ K/W}$.

The role of the heat capacitance can be easily seen in Figure 11. For a pulsed voltage signal of amplitude (peak to peak) = 0.025 V, offset = 0.0125 V and $f = 0.5 \text{ GHz}$ applied in an ideal device whose resistance is assumed to be $R_{RRAM} = 1 \Omega$, the temperature can be obtained from Equation (27) for $R_{th} = 2 \times 10^5 \text{ K/W}$ and $C_{th} = 0.1 \text{ fJ/K}$ ($\tau_{th} = 20 \text{ ps}$), $C_{th} = 0.25 \text{ fJ/K}$ ($\tau_{th} = 50 \text{ ps}$), $C_{th} = 0.5 \text{ fJ/K}$ ($\tau_{th} = 100 \text{ ps}$).

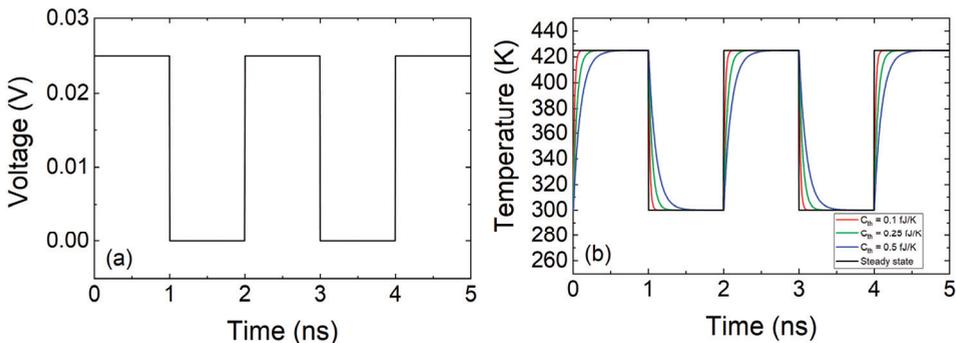


Figure 11. (a) Voltage applied to the device versus time, (b) Temperature versus time obtained for different values of C_{th} (assuming $R_{th} = 2 \times 10^5 \text{ K/W}$).

As can be seen in the previous figure, the device thermal response should be faster than the electric pulses employed for an operation free of delays (“inertia”) due to thermal effects. In fact, experimental techniques have been developed to estimate the device temperature with the application of ultra-short electrical pulses to RRAMs [97,98].

We have made use of some of the thermal models reported above. They cannot exist on their own since the conductive filament kinetics need to be considered to describe the device RS operation and, in doing so, calculate the current. The use of the thermal models TM1-TM4 has been presented previously in [27,56,79]. We show here some results of the Stanford model [78,88,93,95] along with the thermal models TM5 and TM6. For the device description, taking into consideration that no experimental data fitting is considered (since it was performed in the references where the models were introduced), we assumed a set of model parameters close to the one suggested in [88], see Table 2.

Table 2. Model parameters employed for the simulations performed with the Stanford model, in particular for Figures 12 and 13.

Stanford-PKU Model Parameters			
Device Parameters	Unit	Resistive Switching	
		SET	RESET
V_o	V	0.4	
I_0	mA	0.2	
g_0	nm	0.35	
v_0	m/s	10^6	
α	-	1	
β	-	3	
γ_0	-	10	

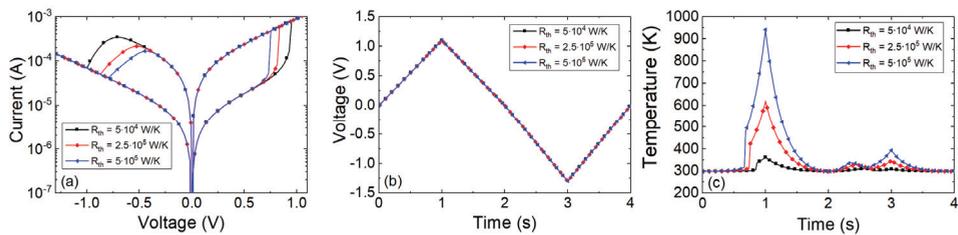


Figure 12. Simulations performed making use of the Stanford model including the TM5 with different thermal resistances. (a) Current versus voltage applied to the device, (b) voltage signal applied to the device, (c) temperature versus time.

Several I-V curves were plotted in Figure 12 considering different thermal resistances. As can be seen, the main dissimilarities are found in the set and reset regions. For the Stanford model, the highest temperatures are found in the set process, see that the Joule heating is higher in the set process and in the interval of positive voltages above V_{SET} . This is coherent with experimental findings that show that the Joule heating role is essential to describe the SET kinetics [81,99]. On average, these maximum temperatures achieved are in line with the estimations performed above for the thermal resistances considered. It is important to highlight the importance of the thermal resistance in the device design. See that higher R_{th} values lead to lower set and reset voltages to produce RS, and hence, lower power consumption. From this viewpoint, higher thermal resistances (i.e., devices showing a character thermodynamically more adiabatic with respect to the surroundings) might be more interesting. Since the heat flux from the CF to the metallic electrodes (operating these as heat sinks, a reasonable assumption, allows to calculate the heat flux with the

material 3D thermal conductivity) could be in the same order of magnitude for different RRAMs, the dielectric could be the key (save the role of the contact thermal resistance). In this respect, we have to call the reader's attention to the fact that the usual RRAM dielectrics are grown in nanometric layers; consequently, the real thermal conductivity due to phonon quantization is far from the values corresponding to the corresponding 3D dielectric materials, as it was shown in [100–102].

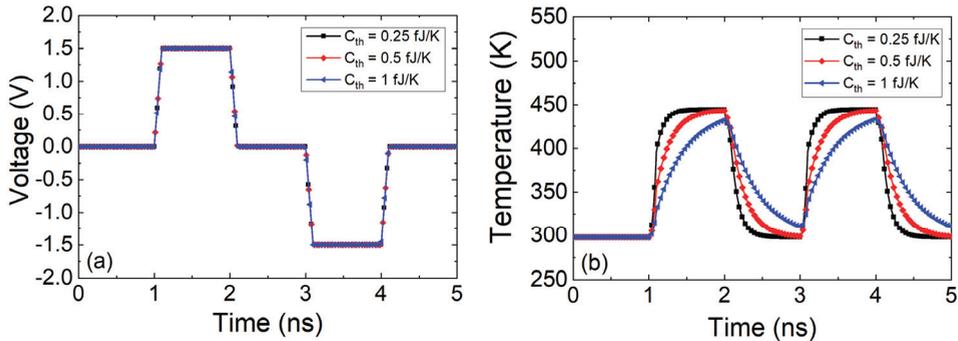


Figure 13. Simulations performed with the Stanford model (including TM6) making use of different thermal capacitances, C_{th} , assuming a common value of the thermal resistance, $R_{th} = 4 \times 10^5$ K/W. (a) Voltage applied to the device versus time, (b) Temperature versus time.

In the case of TM6 along with the Stanford model (using Table 2), we have plotted the results of a simulation using a pulsed voltage signal in Figure 13. A voltage signal such as the one in Figure 12b is close to DC, therefore the use of TM6 instead of TM5 is irrelevant. However, if a fast voltage signal is employed (Figure 13a), a high enough thermal capacitance makes a difference in terms of the device temperature transient (see Figure 13b).

The thermal time constants (Equation (22)) produced obvious delays for a voltage signal such as the one in Figure 13. These delays could seriously affect the device operation under pulsed input signals since RS is most of the times linked to thermal effects [1,24,53,81,99]. The thermal time constants corresponding to Figure 13b are the following: 0.4, 0.2 and 0.1 ns. These values are large compared to the value (33 ps) given by Ielmini [18] (we do not go into details of device materials at this point). An estimation of the C_{th} associated to a CF in a conventional RRAM, as described in [18], could help to shed light on this issue. Let us assume a cylindrical CF radius of 5 nm in a dielectric layer of 20 nm thick, if the heat capacity of Hf is considered ($C_p = 1.92$ JK⁻¹cm⁻³) the CF thermal capacitance would be ($C_{th} = C_p t_{ox} A$) 0.003 fJ/K. Therefore, a value $\tau_{th} = 1.2$ ps is expected for the same thermal resistance employed in Figure 13. Although this thermal time constant is short, different authors [78,95] have used thermal capacitances values that lead to devices with higher thermal constants. A thermal device model described by Equation (20) and the thermal capacitance of an average CF produces so low thermal time constants that no transient term in Equation (20) would be worth being taken into account. From the experimental viewpoint, no delays linked to thermal inertia would be seen for conventional memory pulsed signals. Nevertheless, current transients on longer time scales than the previously calculated τ_{th} , linked to some extent to thermal effects have been reported previously [78]. In this respect, the thermal model, i.e., Equation (20), might not be enough to accurately describe RRAM thermal response.

The coupling of the CF temperature to a heat sink at room temperature with just two parameters (thermal resistance and capacitance) could not be described by the thermal features of a nanometric CF. We could use an intermediate temperature corresponding to an average region surrounding the CF that could help to build two different thermal

circuits, one accounting for the coupling between the CF and this intermediate surrounding region (it could include the dielectric and electrode zones closer to the CF), and a second one coupling between this intermediate region and the outside world. This is in line with previous thermal descriptions (although introduced in another context) employed for magnetic current sensors [103] and AlGaAs/GaAs HBTs [104]. For this purpose, we present the following model. We will show below that the model based on Equation (20) can be used if a thermal capacitance that accounts for the whole device is taken into consideration. This means using a parameter much higher than the exclusively associated to the CF. In doing so, as always in compact modeling, the simplicity and accuracy trade-off has to be considered.

2.4.3. Non-Steady-State Approach with Two Different Temperatures Associated to the Device (Second-Order Memristor)

This thermal model, as suggested above, employs two different temperatures to describe the device from an energy balance perspective: the internal device temperature (approximately the CF temperature, T) that affects the RS mechanisms linked to the CF creation and destruction and a second temperature, associated to the CF surrounding regions (an effective temperature, T_s). The latter influences the internal device temperature T but it shows a different time evolution. The device intermediate surrounding region (at temperature T_s) is characterized by an outer boundary assumed to be at room temperature ($T_0 = 300$ K). This outer boundary is considered to be far away from the RS active region. The intermediate surrounding region can include different material layers; therefore, effective thermal constants are employed to account for the heat flux between this region and the exterior zone. Besides, the coupling between the inner (CF volume) and the intermediate CF surrounding region could be modeled by an effective thermal resistance and thermal capacitance: R_{th1} and C_{th1} . Under this approach, the device can be described by the following two equations (we assume this procedure to be the thermal model 7, TM7; see the circuital implementation in Figure 14).

$$C_{th1} \frac{d(T - T_s)}{dt} = V(t)I(t) - \frac{1}{R_{th1}}(T - T_s) \tag{30}$$

$$C_{th2} \frac{dT_s}{dt} = V(t)I(t) - \frac{1}{R_{th2}}(T_s - T_0) \tag{31}$$

where $V(t)I(t)$ allows the determination of $\dot{e}_{generated}$. The power dissipated by Joule heating affects the intermediate surrounding region temperature (modeled with parameters R_{th2} and C_{th2}) that accounts for the coupling between this region and the thermalized device exterior region. The approach described here is in line with the description of a second order memristor [100].

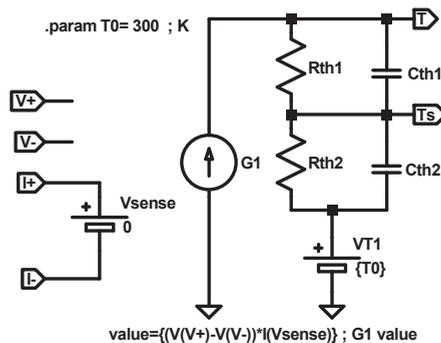


Figure 14. Equivalent electric circuit of a RRAM thermal model based on a double thermal circuit described by Equations (30) and (31).

The simulation was performed with this thermal model integrated in the Stanford compact model that was employed previously, see Figure 15.

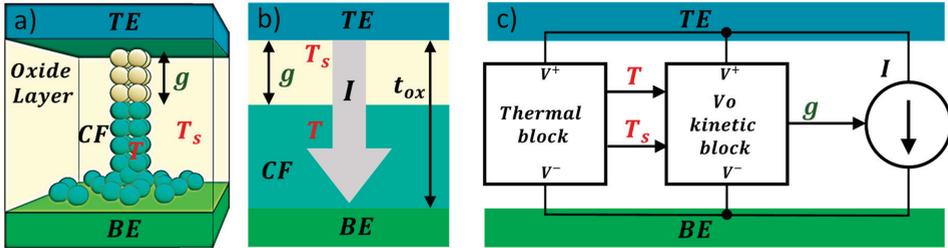


Figure 15. (a) Three-dimensional view of the Stanford scheme to model the different device areas (TE: top electrode, Oxide Layer, CF: conductive filament and BE: bottom electrode), (b) model parameters, g : gap between the TE and the filament tip and t_{ox} : dielectric thickness, (c) subcircuit representation for the implemented model. The connection between blocks represents the states variables used: g , which depends on kinetic block and it is linked to the two temperatures (T, T_s).

The results obtained for the set of parameters of the standard Stanford parameters [88] and the thermal model shown in Figure 14; Figure 15 are given in Figure 16.

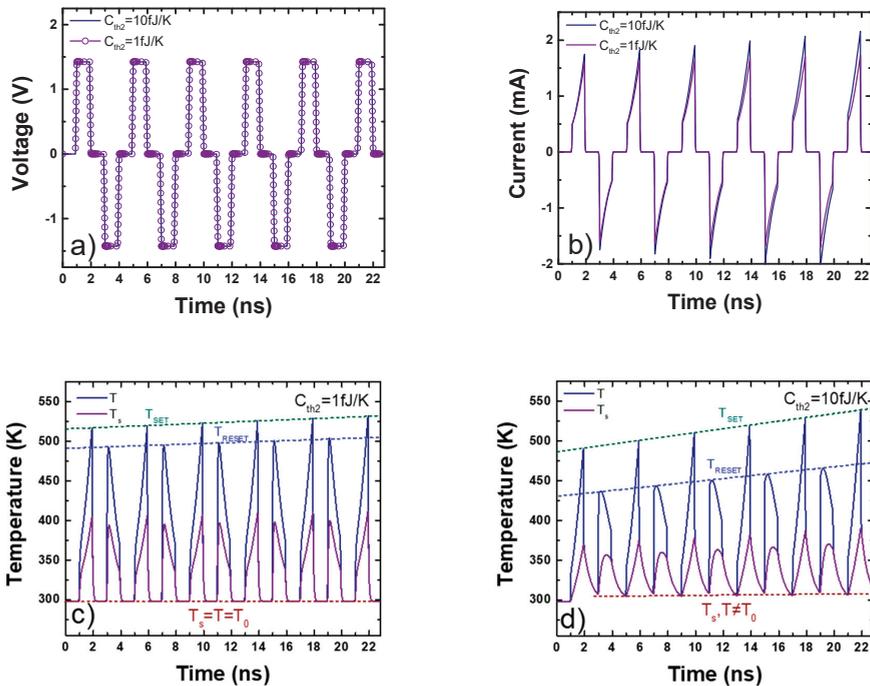


Figure 16. RRAM simulation making use of the Stanford model including a double RC thermal model $R_{th1} = 40 \text{ kK/W}$, $R_{th2} = 40 \text{ kK/W}$, $C_{th1} = 0.003 \text{ fJ/K}$ and C_{th2} with values 1 fJ/K and 10 fJ/K . (a) Applied voltage pulses for consecutive set and reset, (b) temporal current evolution, (c) temporal evolution of device filament temperature (T) and the intermediate surrounding region (T_s) with $C_{th2} = 1 \text{ fJ/K}$ and (d) $C_{th2} = 10 \text{ fJ/K}$.

Depending on C_{th2} , different CF and intermediate surrounding region temperatures transient responses are obtained, producing the corresponding effects on the device current. This is noticeable when a consecutive series of set and reset pulses are applied, as shown

in Figure 16a, in which a sequence of set pulses (1.5 V with 1 ns on time and 0.1 ns rise and fall times) and reset pulses (−1.5 V with 1 ns on time and 0.1 ns rise and fall times). In the first configuration, with the thermal capacities $C_{th1} = 0.003$ fJ/K, $C_{th2} = 1$ fJ/K and thermal resistances $R_{th1} = R_{th2} = 40$ kK/W, the current evolution is shown in Figure 16b. Figure 16c shows the CF (T) and intermediate surrounding region (T_S) evolution. In this first configuration, the corresponding transient shows low thermal inertia; after the pulse application, both temperatures reach room temperature ($T = T_S = T_0$). The devices show a slight increase in the maximum temperatures obtained in the set (T_{SET}) and reset (T_{RESET}) processes (Figure 16c).

In the second configuration, thermal capacities $C_{th1} = 0.003$ fJ/K, $C_{th2} = 10$ fJ/K and thermal resistances $R_{th1} = R_{th2} = 40$ kK/W, the current evolution is plotted in Figure 16b. Figure 16d shows the CF (T) and intermediate surrounding region (T_S) evolution. In this second configuration, the thermal inertia is higher in the second thermal circuit, after each set/reset pulse, the temperatures cannot go back to room temperature ($T, T_S \neq T_0$). As a result, each new cycle starts from a higher temperature than in the previous cycle; therefore, the maximum set (T_{SET}) and reset (T_{RESET}) temperatures show a growing trend (see Figure 16d). This temperature increase over the cycles implies that the device CF gap decreases in each new cycle, then the current increases (Figure 16b). This effect suggests the consideration of the temperature, in addition to the CF gap, as a state variable in line with the approach presented in [100] for second-order memristor. The temperature increase reported above could be employed with a series of pulses to tune the device conductivity in set cycles within a neuromorphic circuit context [100,105,106]. It is noteworthy that a third-order approach has been introduced in modeling devices for neuromorphic engineering [107].

2.4.4. SPICE-Based Circuitual Models with Two or More CF Temperatures

In Section 2.3.4, a compact model based on two different CF representative temperatures was reviewed. In that model, some simplifications were performed in order to obtain analytical expressions for calculating these two temperatures although the flexibility linked to the consideration of different temperatures for the CF narrowing and CF main body added high value to the modeling process. In this section, an approach based on the electrical equivalent representation of this thermal framework is proposed in order to calculate numerically the temperature. It is noteworthy that most of the thermal models based on an electrical equivalent circuit (Sections 2.4.2 and 2.4.3) assume constant thermal resistances and capacitances, which can be used as fitting parameters. However, heat conduction through the CF and lateral heat dissipation depends on the filament size. This effect is included in physically-based simulators, such as those based on a kMC approach or on finite differences/elements, as far as the heat equation is solved using thermal parameters which are updated at simulation time according to the current filament size. Thermal models based on the heat equation analytical solutions in simplified CF geometries (Section 2.3) incorporate also this effect because the temperature analytical expression depends on the actual geometry, and it is evaluated at each simulation time step.

In this section, we present two thermal models based on an equivalent electrical representation (SPICE based), but including the effects of the CF evolution on the thermal properties, which also evolve as the simulation proceeds. The first one is a steady-state model, while the latter includes thermal capacitances. Furthermore, both models account for longitudinal heat conduction and lateral heat dissipation by means of several thermal resistances (or RC networks in the non-steady approach).

Figure 17 shows a general schema of the overall model. As explained before, the temperature of the CF main body is, in general, lower than that of the small portion of the filament where the filament evolves faster. Therefore, the CF is modeled by two different subcircuits (Figure 17), each of them characterized by different state variables (CF radius and temperature).

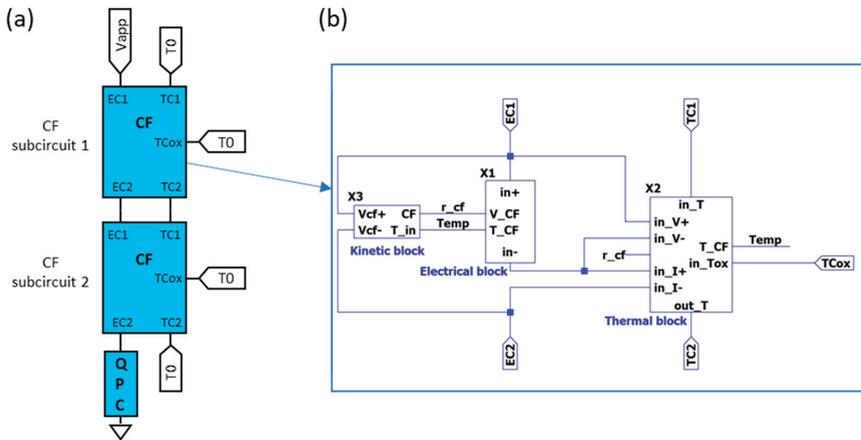


Figure 17. Schema of the circuitual compact model. A truncated-cone shaped conductive filament is represented by connected cylinders for modeling purposes (a). The behaviour of each portion of the filament (cylinder) is modeled by the subcircuit inside the blue rectangle (b), which has electrical connections (EC) and thermal connections (TC). Each cylinder (subcircuit) is characterized by different state variables (radius, r_{cf} , and temperature, Temp). The cylinder subcircuit consists of several more subcircuits: a kinetic block for calculating the transient CF evolution; an electrical block for current calculation; and, finally, the thermal subcircuit, which includes the equivalent circuit for the thermal model. As can be seen, the subcircuits (thermal, kinetic and electrical blocks) are connected all together because they are interdependent. If necessary, a last subcircuit is added in series (a) in order to account for the conduction through a constriction by means of the quantum point contact model (see Section 4) [108].

Now, we focus on the description of the thermal subcircuit (Figure 18). The longitudinal heat conduction is modeled by R_{Thl1} and R_{Thl2} . For the sake of generality, it has been split off into two contributions in order to make easier the connection with other thermal sub-circuits and to build more complex thermal models. Their values are given by [89]:

$$R_{Thl1i} = R_{Thl2i} = \frac{1}{2} \frac{L_i}{k_{th} \pi r_i^2} \tag{32}$$

where k_{th} is the CF thermal conductivity, L_i is the length of the portion of the filament modeled by the sub-circuit and r_i , its radius (index i refers to the cylinder or sub-circuit number 1 or 2 in Figure 17a). On the other hand, R_{Thm} accounts for the lateral heat dissipation and it is calculated following this expression [89]:

$$R_{Thmi} = \frac{1}{2 h L_i \pi r_i} \tag{33}$$

Note that in this model (TM8), the thermal resistances are not directly the fitting parameters since they are calculated according to the actual filament size. Therefore, as far as the complete device model is able to reproduce the geometrical evolution of the filament (kinetic block in Figure 17), the thermal resistances are not fixed, but their values evolve as the simulation runs. The implementation of such dependent resistances can be made by means of behavioural sources.

Although the model shown in Figure 17 uses two cylinders (and the corresponding two sub-circuits), the CF could be represented by more cylinders in order to get a more detailed CF description [31]. Indeed, in the limit with an infinite number of differential length cylinders, the circuit simulation would be equivalent to the resolution of the differential Equation (9). In fact, with a reduced number of filaments, the results are very similar to those obtained with a finite differences simulator [31,109]. Furthermore, complex filaments such as those with several branches forming a tree structure or interlaced between them

could be simulated using more blocks and interconnecting them following a given structure (Figures 5 and 6 in [31]).

On the contrary, if only one block is used, this thermal model (TM8) would be equivalent to TM5, although the thermal resistance evolution is allowed in TM8.

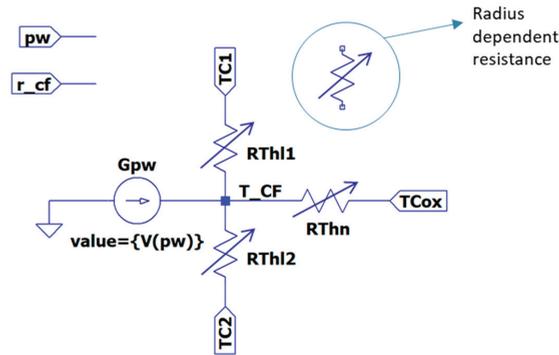


Figure 18. Circuitual equivalent for thermal model TM8. The circuit inputs are the dissipated power (p_w) and the CF radius (r_{cf}), while the output is the temperature (T_{CF}). The actual values of the thermal resistances depend on the filament radius (it is assumed to be a cylinder) and, therefore, they are updated as the CF evolves. The subcircuit has been prepared for being connected to other thermal subcircuits (through TC1, TC2 and TCox) in order to obtain a more complex thermal model of the whole device (with several temperatures along the filament or different temperatures for the surrounding insulator or bulk insulator, Figure 17). If only one block is used, all the resistances are in parallel and the model is equivalent to TM5, although the thermal resistance value keeps the dependency on the filament size in TM8 and it changes during the simulation.

Figure 19 shows the results provided by TM8 when is coupled to kinetic and conductive blocks fitted to simulate reset transitions in unipolar Ni/HfO₂/Si-n⁺ resistive switching devices [80,109,110]. The QPC block has also been added. The two cylinders-TM8 model results have been compared with those provided by a finite differences simulator that was used to fit the experimental data [80]. The lateral heat dissipation parameter, h , has been changed in order to check its influence on the i - v curve. As can be seen, more heat dissipation requires a higher voltage to reach the thermally triggered reset transition, a well-known effect in RRAMs.

Thermal inertia can also be considered following this approach if thermal capacitances are added (Figure 20, thermal model TM9) [37]. In this new model, thermal capacitances could also be made dependent on the filament size instead of being fixed fitting parameters [37,111]. As previously mentioned, several blocks can be connected for modeling the CF. On the contrary, if only one segment is used, the model is equivalent to model TM6 (although TM9 lets the thermal components evolve at simulation time).

Figure 21 shows the simulation of the transient response of a Ni/20 nm-HfO₂/Si-n⁺ resistive switching device [110] when a 3 V reset pulse is applied (for 100 ns) [37]. Several values of the thermal capacities have been considered. The simulation context here is different from the one shown in Section 2.4.3 since all the modeling components are linked to the device conductive filaments. Note also that only values higher than 0.2 fJ/K influence the device response. Fixed and variable thermal capacities have been used in order to analyze the role of size-dependent thermal capacities, which evolve at simulation time. As expected, variable thermal capacitors, whose value is reduced during a reset process, produce lower thermal inertia.

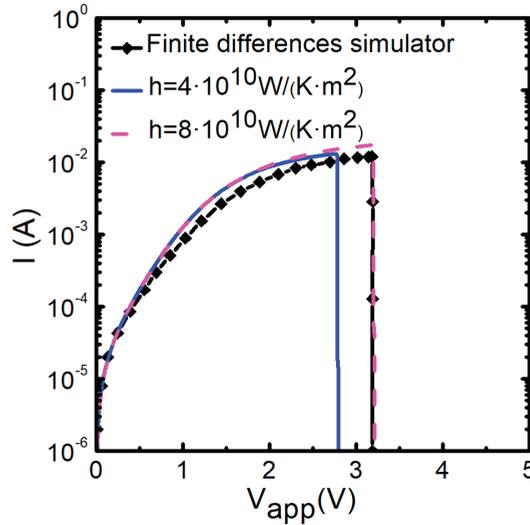


Figure 19. Simulation of a reset transition in unipolar Ni/20 nm-HfO₂/Si-n⁺ resistive switching devices [109]. The *i-v* curve provided by a finite differences simulator used to fit the experimental data [80] is compared with the *i-v* curve calculated by means of the two cylinders model with TM8. Note that with only two subcircuits (Figure 17a) and taking variable electrical and thermal resistances into account, both types of simulators provide very close results, as far as the circuitual model includes variable electric and thermal resistances. Two values of the lateral heat dissipation parameter, *h*, have been used for the sake of comparison.

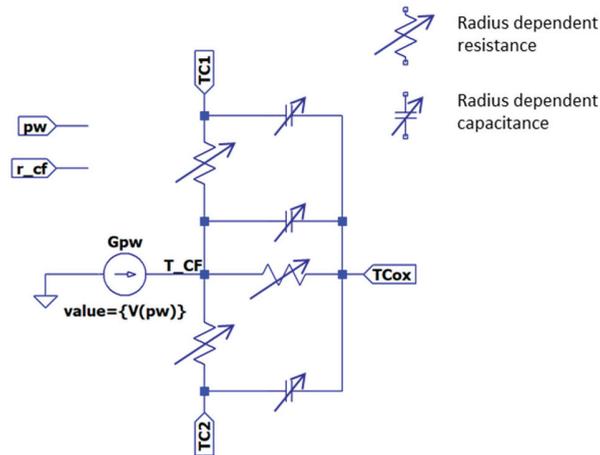


Figure 20. Circuitual equivalent for thermal model TM9. It is similar to TM8 (Figure 18), but thermal inertia has been added by means of capacitances. As in TM8, the actual values of the thermal resistances and capacitances depend on the filament radius (it is assumed to be a cylinder) and, therefore, they are updated as the CF evolves [37].

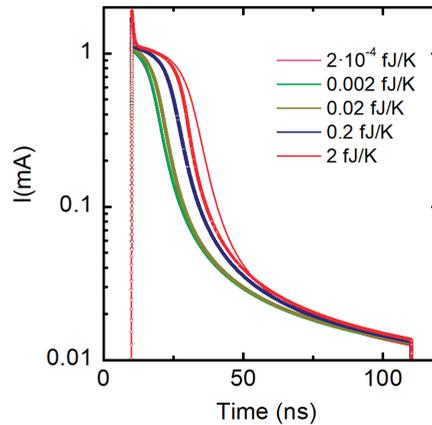


Figure 21. Simulated current in a Ni/20 nm-HfO₂/Si-n⁺ resistive switching device [37,110] when a 3 V reset pulse is applied (for 100 ns). Different values of the thermal capacities have been assumed. Fixed thermal capacitances (solid lines) and size-dependent thermal capacitances (symbols) have been used [37,111].

Finally, it was previously seen that TM7 deals with two temperatures (at the filament and at the surrounding insulator). Note that although TM9 (following the two cylinders schema shown in Figure 17) also consider two temperatures, they are both linked to the conductive filament. TM7 can be obtained as a particular case of TM9 considering only one cylinder, but connecting another RC network between the node *TCox* and a voltage source for representing the bulk insulator temperature. It is important to note that in the TM9 case, variable (at simulation time) thermal components are allowed.

3. General Memristor Modeling Framework with Thermal Effects Emphasis

In this section, a different approach to model RRAM thermal features is proposed. For this purpose, we make use of the general memristor modeling workspace that was introduced by Corinto and Chua in [71]. This alternative perspective complements the developments presented in the previous section. In particular, the authors [71] developed a unified theoretical framework and also discussed the advantages of using the flux-charge (φ - Q) domain to study memristor elements. Within this framework, memristors, in the taxonomy proposed in [72] (the ideal, the generic, and the extended memristor), are described as the result of different approximations in the equations. This extended categorization emerged as a necessity in order to include theoretically the description of pinched, hysteretic behaviours demonstrated by various elements, not only in circuit theory and electronics but also in nature.

Among the different categories presented above, the most general class is linked to extended memristors, which refers to memristors that have extra state variables (in addition to φ and Q). For the specific case of charge-controlled memristors, they are described by the following equations:

$$v = M(Q, i, \mathbf{X}) i \quad (34)$$

$$\frac{d\mathbf{X}}{dt} = g_Q(Q, i, \mathbf{X}) \quad (35)$$

$$\frac{dQ}{dt} = i \quad (36)$$

The memristance M of an extended memristor is implied in Equation (34), apparently bearing the feature of nonlinearity; v is the voltage across the memristor, i is the current flowing through it, and Q is the charge, i.e., the current first momentum. The vector \mathbf{X} stands for a set of extra state variables, including all the necessary physical magnitudes

according to the implemented memristive system; indicatively, they could be the device internal temperature, the conducting filament radius, or any other non-electrical variable influencing the memristor state that ultimately affects the device charge conduction. Apparently, the dynamics of the state variables X are governed by $g_Q(Q, i, X)$ and Equation (35). It is noted that the importance of the class of extended memristors comes from the fact that all real-world memristor devices known until now are indeed extended memristors. Notice that from Equation (34), we can define the memristance as follows:

$$M(Q, i, X) = \frac{v}{i} = \frac{d\varphi/dt}{dQ/dt} = \frac{d\varphi}{dQ} \quad (37)$$

where φ is the voltage first momentum, usually called flux in analogy with the charge. See, however, that a more useful way to obtain this relation is through derivation by assuming that the charge and the flux are related by a function f :

$$\varphi = f(Q, i, X) \quad (38)$$

Then, by deriving with respect to time, and using the chain rule, we obtain:

$$\frac{d\varphi}{dt} = v = \frac{\partial f(Q, i, X)}{\partial Q} \frac{dQ}{dt} + \frac{\partial f(Q, i, X)}{\partial i} \frac{di}{dt} + \frac{\partial f(Q, i, X)}{\partial X} \frac{dX}{dt} = \frac{\partial f(Q, i, X)}{\partial Q} i = \frac{\partial \varphi}{\partial Q} i \quad (39)$$

The latter part of Equation (39) is obtained under the assumption [71] described below,

$$\frac{\partial f(Q, i, X)}{\partial i} \frac{di}{dt} + \frac{\partial f(Q, i, X)}{\partial X} \frac{dX}{dt} = 0 \quad (40)$$

The system memory capability under no excitation is determined by a special case of Equation (35), often referred to as the power-off plot (POP) equation; in this case we have $i = 0$ or equivalently $Q = \text{constant}$. If a single state variable is considered, it is clear that if the POP equation is nil under these conditions, the system presents then a long-term memory since the state variable will not change with time; while if it is different to zero, the system is capable of exhibiting only short-term memory.

The consideration of the temperature, T , as the state variable is a peculiar case since there is an influence from external sources (i.e., the ambient –room– temperature, T_0); this implying a possible energy input in some cases if T_0 is not constant. In addition, as it has been discussed in Section 2, it is difficult to determine a single value for the device internal temperature (some models, as shown above, include two different temperatures to better describe the device operation). We can write the equations by separating the temperature as follows:

$$v = M(Q, i, X, T, T_0) i \quad (41)$$

$$\frac{dX}{dt} = g_Q(Q, i, X, T, T_0) \quad (42)$$

$$\frac{dT}{dt} = g_T(Q, i, X, T, T_0) \quad (43)$$

These equations include both temperatures: the internal device temperature, T , and the external T_0 . Obviously, there is no equation governing T_0 dynamics since it can be considered as an external signal. Temperature, T , may be a position-dependent temperature $T(x, y, z)$, as already presented in Section 2.1. In this case, Equation (43) would correspond to the heat equation. As an additional note, it is important to highlight that a device will not present long-term memory characteristics associated solely with temperature, since the device will tend to reach thermal equilibrium with the external medium. In absence of any external electrical input, this would mean that the POP equation related to the evolution of the internal temperature is not zero in the general case. This does not preclude, however, that the system may have other internal variables that do present a long-term memory capability. As an example, we can think if the case of a phase change memory (PCM),

where a phase change is activated by temperature, and it remains even after the device has cooled back to room temperature. A similar situation occurs when a RRAM conductive filament is ruptured because of an enhanced diffusion process favored by a temperature rise [24,80].

Example of Application

As an easy example, we can consider the case of the thermistor, which is one of the first elements identified as an extended memristor, i.e., a device whose resistance is dependent on some internal state variable that presents memory effects [112,113]. In this respect, and for the modeling developments henceforth, they display parallelism with RRAMs.

The model has been known since Steinhart and Hart published a function which fitted the variation of thermistor-resistance according to temperature [114] as a Taylor's expansion of the device conductance in terms of the temperature logarithm. This function, along with the equivalent Ohm's law in Equation (44), has proved to be suitable in a wide variety of thermistors, for ranges from a few degrees to a few hundred degrees, and it has been widely used to model this kind of devices when used as temperature sensors. The most usual way to describe it is by means of a simplification shown in Equation (45). In addition, a key thermistor characteristic is linked to self-heating, which can be described by Equation (46), by neglecting radiative heat dissipation:

$$v = M(T, T_0) i \quad (44)$$

$$M(T, T_0) = R_0 \exp\left(B \left(\frac{1}{T} - \frac{1}{T_0}\right)\right) \quad (45)$$

$$\frac{dT}{dt} = \frac{R_0 i^2}{C} - \frac{\delta}{C}(T - T_0) \quad (46)$$

In the above equations, T_0 is the room temperature, and T the device internal temperature. The rest of the symbols are parameters of the thermistor model and can be considered as constants for all practical purposes. At this point, it is noteworthy to point out that these equations bear exactly the same form as Equations (41) and (43) and, thus, identify the thermistor as a memristor. That is, the thermistor is a device whose resistance depends on its electrical history, and it has an internal state variable that governs the overall behaviour (the device internal temperature). Thus, the device can be classified as an extended memristor.

In addition, if we look at the POP equation (Equation (46) with $i = 0$), we see that the temperature derivative is different from zero for any situation other than the device thermal equilibrium with the surrounding environment. Thus, the device does not possess a feature linked to long-term memory. In this respect, it is also illustrative to point out that there are other memristive systems [115] that are also extended memristors due to self-heating, even if the thermal specific mechanisms are different from those of thermistors.

As an example to illustrate the memristive behavior of this device, we have simulated it when driven by a triangular current waveform, using specific values extracted from a datasheet for the thermistor constants: $\delta = 4 \times 10^{-3} \text{ W K}^{-1}$, $C = 60 \times 10^{-3} \text{ J K}^{-1}$, $B = 3950 \text{ K}$, $T_0 = 298 \text{ K}$, $R_0 = 10 \text{ k}\Omega$. Additionally, and in accordance with a typical thermistor datasheet, we have set a maximum current of 4.5 mA, and we have also used 5 different ramp slopes, as plotted in Figure 22.

Figure 23 plots the evolution of the memresistance as well as the current input versus time. The input signal shown in Figure 22 has been employed as well as the Equations (44)–(46).

In addition, we have also plotted these two magnitudes used in the Y axis previously against each other in Figure 24, showing the effects of the different slopes in the device memresistance.

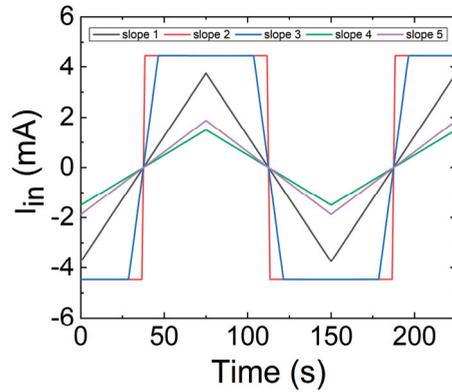


Figure 22. Input current waveform versus time for five different ramps. Colours are coherently employed in the following plots.

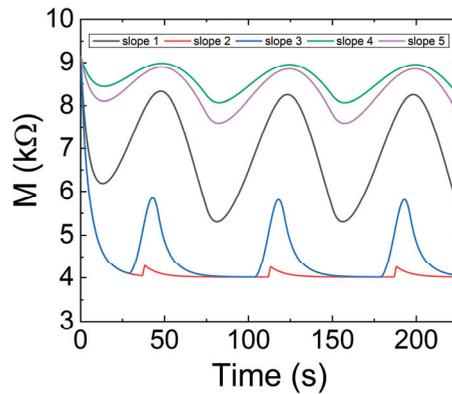


Figure 23. Memristance versus time for five different input voltage signals under ramped voltage stress.

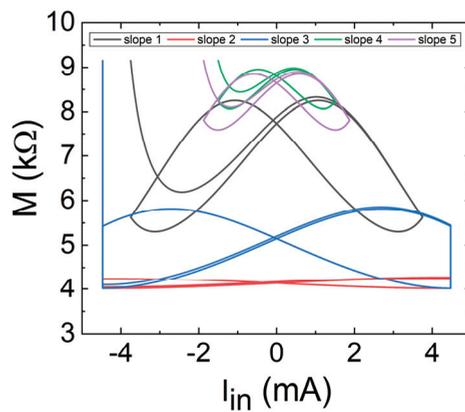


Figure 24. Memristance versus input current, for five different slopes. Colours are coherent with the results shown in the previous figures.

Then, the typical i - v memristor characteristics showing the famous loop are drawn in Figure 25. See that the shapes are in line with what is expected for memristors [71].

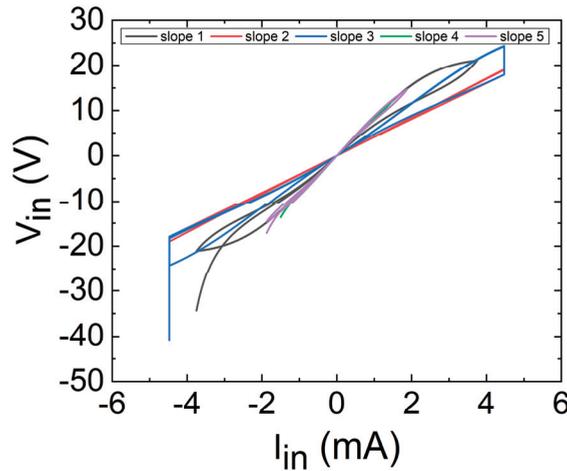


Figure 25. i - v thermistor characteristics for five different input voltages.

Figure 25 shows the two fingerprints of a memristor [116]: (1) a pinched loop; and (2) an area that varies with frequency, tending to a line at high frequencies. In fact, the behaviour at the highest frequency (cyan line) is nearly that of an ohmic resistor, with no loop area, while at lower frequencies the behaviour is different. It has to be noted that (see [115]) the situation is more interesting than simply an area increase at lower frequencies. As highlighted in [115], the thermistor control variable is the internal temperature and it tends to be in thermal equilibrium with the surroundings, which causes the loop area to reduce at a very low frequency. As we use it in the corresponding equations, we can see that for very low input signal slopes, the device always reaches thermal equilibrium, since the dT/dt is nearly zero, and its behaviour tends to be close to a nonlinear resistor, as shown in Figure 24; Figure 25 (red lines), with a null area enclosed in the loop.

At this point, the concept of dynamic route map (DRM) [36] comes up since it is quite useful to represent the device time evolution (again, in this facet, a full parallelism with RRAM is observed [36]). In fact, the DRM is a concept arising from non-linear dynamical systems, and represents the trajectories a system follows in the phase space of the state variable versus its derivative for different control parameter values. If we plot it as a 3D diagram, we find that all the trajectories, for a given constant T_0 , are bound to fall on the same surface, as seen in Figure 26. Using this representation may provide very interesting insights into the device dynamics. Considering our thermistor, if a trajectory goes from a state with positive derivative to another characterized by a negative derivative with increasing temperature, then it will reach a stable equilibrium point at the temperature where the derivative nullifies. An equilibrium point is a state where the device tends to remain at even if it drifts from it in its operation; this idea resembles a similar concept related to the DC quiescent point in circuit theory, or memory in memristors. In the opposite case, when the trajectory goes from negative to positive, an equilibrium point might seem to come up at the zero-crossing temperature, but it is unstable, which means that the slightest change will force the system to come out of it.

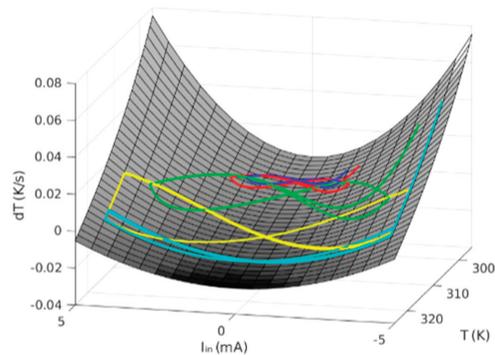


Figure 26. Memristor Dynamic Route Map (surface), showing as lines the five trajectories corresponding to the previous figures, using the same colour code. It can be seen that all these trajectories fall on the surface, which defines univocally the device behaviour. Notice that this surface is, in fact, a family of surfaces that depend on the room temperature T_0 .

4. RRAM Quantum Point Contact Modeling, Thermal Effects

So far, we have studied thermal effects from a classical physics viewpoint. This is the approach commonly used in most compact models. However, the scale of the material layers that form part of a RRAM makes feasible for certain devices and for particular operation conditions the observation of quantum effects. In particular, when the conducting filament (CF) cross-sectional area in a RRAM device becomes very narrow, only a few atoms wide, the continuum description is expected to break down, so that the direct application of the heat equation becomes questionable [117,118]. We enter into the regime of heat transport and dissipation at the nanoscale [119]. Before starting with a discussion about these topics, it is important to discriminate between the role that temperature plays on the ion/vacancy movement across the insulating films (essentially governed by Kramers' theory [120]), and the temperature dependence of the mechanism adopted for the electronic transport in the CF itself (Schottky, Poole-Frenkel, tunneling, variable range hopping, space charge limited conduction, quantum point contact, etc.) [121]. Although both descriptions are intrinsically connected and they are at the heart of the complexity of the RRAM behavior, they are often treated separately for simplicity, or one of them completely dropped. To deepen into these intertwined approaches, a detailed RRAM dynamic simulation at the microscopic level is imperative. Ion/vacancy diffusion process, which defines the filamentary structure, depends on temperature, and the size of the structure determines the magnitude of the electron current that governs the power dissipation (Joule heating effects), which in turn affects the local temperature that drives the diffusion process. In this section we will exclusively focus the attention on the modeling of the electron transport at the nanoscale and the influence of temperature and power dissipation on it. The role of ions/vacancies will be indirectly addressed (more on this issue is explained in Section 5). Temperature evolution in the structures under study (e.g., Figure 1; Figure 2) is extensively covered in Section 2. First, a fixed ion/vacancy arrangement will be considered for simplicity, so that two particular extreme cases, LRS and HRS, will be examined. Second, a phenomenological model for the transition from HRS to LRS which takes into account the power dissipated at the CF bottleneck will be presented. As already discussed previously, while in LRS, the CF is completely formed establishing a metallic-like connection in between the electrodes; in HRS, the filament presents a gap along its structure as a consequence of the absence of conduction states [122]. Thereby, a common theory for both cases able to demonstrate consistency with the experimental observations is required.

Mesoscopic physics, a subdiscipline of condensed-matter physics, has resulted in a suitable framework for semi-empirically describing the temperature dependence of the

electron flow in narrow constrictions and, in particular, in RRAMs. Mesoscopic physics describes the conducting properties of systems whose size lays in between the macroscopic (bulk material) and the microscopic (atoms and molecules) worlds. Since we are talking about atomic dimensions, quantum mechanics is at the foundations of mesoscopic physics [123]. Within this framework, the quantum confinement associated with filamentary conduction is described in terms of the electrochemical potential, potential wells, potential barriers, and bands (valence, conduction, gap). We also talk about a semi-empirical approach because the local temperature is frequently unknown and the external temperature is considered as a control parameter. This objection can be partly overcome if models including two different temperatures (for the cold and hot part of the CF, and for the CF and its surrounding region, see Sections 2.3.4 and 2.4.3) are employed. The idea of using a mesoscopic approach is the consequence of the observation of experimental RRAM conductance values around integer and non-integer multiples of the quantum conductance unit $G_0 = 2e^2/h$, where e is the electron charge and h the Planck's constant [124]. In terms of resistance, this unit is $R_0 = 1/G_0 = 12.9 \text{ K}\Omega$. The experimental conductance values for many cycles measured at a fixed bias, or the conductance measured at consecutive steps in one cycle at different or constant biases are often displayed using histogram plots with the x-axes normalized to G_0 . In many cases, these histograms reveal a peak structure which is interpreted as an indicator of the number of channels available for conduction or as the occurrence of preferred atomic configurations for the CF [125]. Although the detection of peaks in the device histograms is recognized as the signature of quantum point-contact conduction, it should be taken into account that measurements can be seriously affected by a number of factors such as the existence of multiple conduction paths, series resistance, roughness and scattering caused by the granularity of matter, in general, non-adiabatic (non-smooth) potential profiles. Caution should also be exercised with the use of the term *conductance quantization*: only for simple s -electron metals, the transmission probability for the conductance channels is expected to open close to integer values [126]. For this reason, observations in the field of RRAM should be more appropriately considered to be in the quantum (rather than in the quantized) regime of conductance [125].

Many experimental results on resistive switching materials have been interpreted in terms of conduction through atom-sized filamentary structures [127]. This is the case of a wide variety of binary and ternary oxides such as SiO_x [128–131], HfO_2 [132–139], Ta_2O_5 [140–142], NiO [143,144], ZnO [145,146], $a\text{-Si:H}$ [147], TiO_2 [148], V_2O_5 [149], YO_x [150], and BiVO_4 [151]. Nonlinear effects in HfO_2 were also reported by Degraeve et al. [152] and in $\text{CeO}_x/\text{SiO}_2$ -based structures by Miranda et al. [153]. From the point of view of theory, it is worth mentioning that the CF formation in monoclinic- and amorphous- HfO_2 was investigated from first principles by Cartoixa et al. [154] and by Zhong et al. [155]. The filamentary paths are built from oxygen vacancies and using a Green's function formalism coupled to a density functional theory code, the conductance of filaments of different lengths was calculated. According to the obtained results, even the thinnest CFs can sustain conductive channels exhibiting signs of quantum conduction.

Very often, LRS is associated with conductance values $G \geq G_0$ and with a linear I - V curve (not to be confused with Ohmic behavior). In this case, the device conductance can reach values from 10 to 100 times G_0 which indicates the large number of atoms participating in the filament formation. On the other hand, HRS is associated with conductance values $G < G_0$ and with a non-linear I - V curve (mainly with exponential behavior). This state is characterized by a gap or potential barrier which acts as a blocking element for the electron flow. As the starting point for the inclusion of the thermal effects in RRAMs, the Buttiker-Landauer approach for quantum point contacts is considered [156]. Importantly, the analysis does not discriminate between CBRAMs and OxRAMs, so they are treated on equal grounds.

According to the finite-bias Landauer’s formula [157], the I - V characteristic of a mesoscopic conductor can be expressed as:

$$I = \frac{2e}{h} \int D(E)[f(E - \beta eV) - f(E + (1 - \beta)eV)]dE \tag{47}$$

where E is the energy, D the tunneling probability, f the Fermi-Dirac (FD) distribution function, and $0 \leq \beta \leq 1$ the fraction of the applied voltage that drops at the source side of the constriction. For a symmetrical structure $\beta = \frac{1}{2}$. Assuming an inverse parabolic potential barrier for the constriction bottleneck, D is given by [158]:

$$D(E) = \{1 + \exp[-\nu(E - \varphi)]\}^{-1} \tag{48}$$

where ν is a coefficient related to the curvature of the potential barrier and φ the height of the potential barrier that represents the confinement effect (see Figure 27). For $T = 0$ K, (47) and (48) yield [159] (see Figure 27):

$$I(V) = G_0 \left\{ V + \frac{1}{e\nu} \ln \left[\frac{1 + \exp[\nu(\varphi - \beta eV)]}{1 + \exp[\nu(\varphi + (1 - \beta)eV)]} \right] \right\} \tag{49}$$

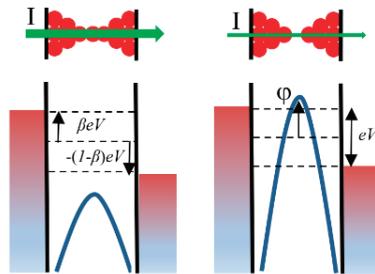


Figure 27. Schematic of the energy structure of the conducting filament. In LRS (high current), the CF is completely formed and the confinement potential barrier is low. In HRS (low current), the filament is broken and the confinement potential barrier is high. The green arrows width indicates the electron current magnitude.

Figure 28 shows some typical modeling results using Equation (49). Any additional potential drop along the confinement structure can be accounted for using the transformation $V \rightarrow V - I R_S$ in (49), where R_S is a series resistance. Equation (49) can be modified so as to include many parallel conducting channels [138]. For LRS, we can consider that there is no blocking element along the CF so that assuming $\varphi \rightarrow -\infty$ ($D \rightarrow 1$) in (49), we obtain:

$$I(V) = G_0 V \tag{50}$$

which is the celebrated Landauer formula for a monomode ballistic conductor [160]. Following [134], the temperature dependence can be introduced into (50), assuming $R_S(T) = R_{S0} \cdot [1 + \alpha_T(T - T_0)]$, where $R_{S0} = R_S(T_0)$, α_T is a temperature coefficient, and T_0 the room temperature. In this case, the I - V characteristic still follows a linear relationship but with a lower slope given by:

$$I(V) = \frac{G_0}{1 + G_0 R_S(T)} V \tag{51}$$

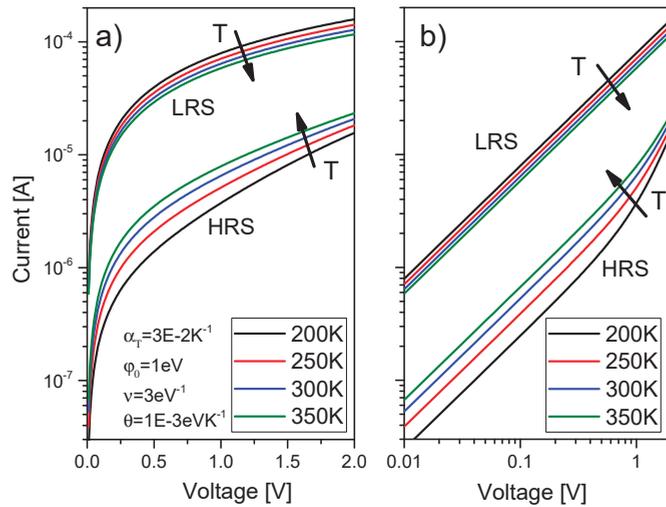


Figure 28. Effects of the temperature on the HRS and LRS I-V characteristics. (a) log-linear axis and (b) log-log axis.

If α_T is a positive coefficient, as expected for a metallic-like conductor, the current decreases as the temperature increases (see Figure 28). This behavior is in agreement with the experimental observations [134]. Notice that here the emphasis is put on the connection of the ballistic region with the rest of the device (internal or external) and in particular with the contacts. Nevertheless, R_S can also be viewed as the momentum relaxation factor along the filamentary structure. If we move to the opposite limit, for HRS, and we consider specifically the case $E \ll \varphi$, (48) reads:

$$D(E) \approx \exp[v(E - \varphi)] \tag{52}$$

so that (47) can be integrated taking into account the temperature-dependent smearing of the FD distributions at the contacts. The result is [161]:

$$I(V) \approx \frac{2e}{h\nu} \frac{\exp(-v\varphi)}{\text{sinc}(\pi\nu kT)} \{ \exp[v\beta eV] - \exp[-v(1 - \beta)eV] \} \tag{53}$$

which provides the exponential behavior observed for HRS. Now, notice that the temperature appears explicitly in (53) through the *sinc* function. In this case, the current increases with the temperature as expected from the availability of more energetic electrons at the injecting electrode. However, it can be shown that for a set of typical fitting parameters, the smearing of the FD functions is not enough to account for the observed temperature effects in HRS. In order to circumvent this problem, a new parameter is introduced into the model Equation (53) so that a larger variation of the current can be achieved. Following experimental observations for the soft breakdown conduction mode in SiO₂ [161], the confinement potential barrier height φ can be parameterized as $\varphi(T) = \varphi_0 - \theta(T - T_0)$, where $\varphi_0 = \varphi(T_0)$ and $\theta > 0$ is a linear temperature coefficient. This correction term arises from the thermal movement of ions/vacancies in the CF around their equilibrium positions. In this case, as the temperature increases, the tunneling current increases because of the reduction of the effective barrier height (see Figure 28). The temperature effect on the barrier profile was recently investigated in detail in [139] using inverse modeling in combination with the WKB approximation for the tunneling probability.

To conclude this section, it is worth mentioning that according to the standard theory of mesoscopic devices, heat largely dissipates at the electrodes (reservoirs) and thermal

and electrical conductances are proportional through the Wiedemann-Franz law [119]. This idea is to heuristically explain why a CF of atomic dimensions is able to reach a stationary current state with conductance values of the order of G_0 . Notice that the current density flowing through a nanoscale CF can be extraordinarily high. The question can be summarized as, where is power dissipated in a RRAM system exhibiting quantum properties? This is a fundamental question in mesoscopic physics [123]. Let us consider here the progressive increase of the current flow as a function of time when the device is subjected to a constant voltage stress after electroforming. This process corresponds to the transition HRS→LRS which arises because of the CF widening. Following [162], we can write first the following phenomenological equation for the current evolution:

$$\frac{dI}{dt} = \eta P_C \quad (54)$$

where η is a temperature- and material-dependent coupling coefficient and P_C is the power dissipated at the constriction bottleneck. For the simplest case of a constant applied bias V , Equation (54) expresses that the current levels off in the long run because power dissipation first increases and then progressively transfers from the constriction to the electrodes. Second, according to Landauer's formula, the transmission probability D (average) can be expressed as a function of the current flowing through the structure as:

$$\tilde{D} = G_0^{-1}G = (G_0V)^{-1}I \quad (55)$$

and the power dissipated at the constriction can be calculated from the voltage drop V_C occurring at the constriction using:

$$P_C = V_C I = V \left(1 - \tilde{D}\right) I = VI \left(1 - \frac{I}{G_0V}\right) \quad (56)$$

Then, from expression (54), an explicit differential equation for the current evolution is obtained:

$$\frac{dI}{dt} = \eta VI \left(1 - \frac{I}{G_0V}\right) \quad (57)$$

Equation (57) is nothing but the logistic equation with effective transition rate ηV and carrying capacity G_0V . The solution to Equation (57) for a constant bias reads:

$$I(t) = \frac{G_0 I_0 \text{Exp}(\eta V t)}{I_0 [\text{Exp}(\eta V t) - 1] + G_0 V} \quad (58)$$

which complies with $I(t=0) = I_0$ and $I(t=\infty) = G_0V$, the initial and stationary conditions, respectively. Equation (58) expresses that, when a mesoscopic channel with conductance G_0 is formed, the power fundamentally dissipates at the electrodes and not at the constriction's bottleneck (see Figure 29). Power is indeed dissipated at the constriction during the CF formation as discussed in the next section. Of course, this is a simplistic view of a much more complex process.

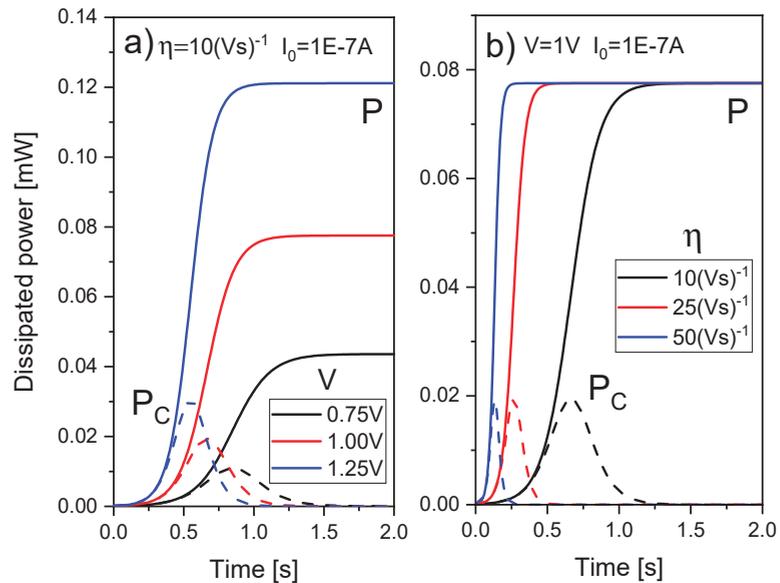


Figure 29. Evolution of the power dissipated in the structure P (solid lines), and at the constriction P_C (dashed lines). (a) Corresponds to different applied voltages V , and (b) corresponds to different transition rates η .

Although most of the models addressed in this manuscript are devoted to devices that show single filamentary conduction, some of them could also be applied to area-dependent devices and even to devices that do not require electroforming [1,2,70]. In particular, the Landauer's approach can be extended to area-dependent devices by assuming multifilamentary conduction. This is the case when the Landauer formula (49) includes a prefactor N dealing with the number of identical filaments assumed [138,159]. In addition, a modeling procedure in line with the general memristor framework presented in Section 3 could also be possible [71,72].

5. Thermometry of Conducting Filaments

In addition to the developments described above in relation to the HE solutions in different modeling approaches and levels of complexity, it is interesting to understand the dielectric breakdown (BD) phenomenon in the context of RRAM operation. In this respect, we shed light in this section on the structural damage that occurs during the BD current transient. In ultra-thin dielectric layers (<5 nm), there is a wide consensus around considering that the intrinsic BD is related to the generation of defects in the dielectric film [163–166]. When the density of bulk defects is high enough, the BD event is triggered by the local connection of the electrodes through a defect related conduction path. Once a defect percolation path is formed, the main feature is a progressive increase of the current across the dielectric. This phenomenon, often referred to as progressive breakdown (PBD), is an universal process that lies under a wide variety of dielectric materials, ranging from traditional oxides, such as SiO_2 , SiO_xN_y [167] to innovative 2D dielectrics, such as h-BN [168], passing through high-k materials such as Al_2O_3 and HfO_2 [169].

The physical structure of the filament formed during the PBD regime has been deeply studied. In the case of poly-Si/SiON/Si MOS devices during PBD, it was demonstrated that the filament is, at least in part, made of Si atoms, through the mechanism of dielectric breakdown induced epitaxy (DBIE) [170,171]. The filament sizes were directly observed by scanning transmission electron microscopy (STEM) after the BD of MIM structures with either Ti/HfO₂/TiN or with Hf/HfO₂/TiN devices, in which the top electrode (Ti

or Hf) acted as cathode. Clear evidence of the formation of a metallic filament made of, respectively, Ti or Hf was reported by using electron energy loss spectroscopy (EELS) imaging [172,173]. In the case of 2D h-BN (CVD) dielectric layers, there is strong evidence that the CFs are formed by metal ions that penetrate from the electrodes into the h-BN stack under the action of the electric field [174,175].

Different experiments have probed that the SET event in RRAM devices [176,177] and the dielectric BD of gate oxides [169,178] have some common aspects. In addition to the clear dependence of the CF characteristics on the maximum current flowing through the device [18,179], TEM imaging of Si-based MOS capacitors prior to and post dielectric BD [163,170,180] and HfO₂-based RRAM cells after forming and cycling [172,181] show comparable microstructural changes in the oxide, suggesting the diffusion of the anodic atomic species into the oxide layer in both cases. Thus, these two phenomena share not only similar electrical characteristics, but also generate comparable microstructural changes, suggesting a common underlying physical mechanism. In such scenario, we propose to model the results for the SET event in RRAM devices similarly to the gate-oxide BD in MOSFETs.

The PBD effect has been captured by the model proposed by Palumbo et al. in [169,182], and later expanded by Lombardo in [183], clarifying the primary role played by the carrier energy loss through the PBD spot. Such model accounts for the physics behind the progressive evolution of the current, where the BD process is closely linked to the energy transfer from the CF itself to its surrounding atomic lattice. According to this idea, the high temperature associated with the localized current flow (being the BD spot area of 1–50 nm², the current density can reach a few MA/cm² [184–186]) would contribute to the generation and enlargement of the BD filament connecting the electrodes of the stack, enabling the promotion of the electro-migration of the fastest available atomic species. Since this technique unambiguously relate the transition rate (dI_T/dt) to the heat dissipation properties during the atomic diffusion of the cathode or anode atoms into the gate dielectric in the region of the percolation path, it is possible estimate the CF temperature. Considering the model reported in [169], we can express the current transition rate (marked as TR) as:

$$TR = \frac{dI_T}{dt} = \frac{q V f_1}{k_B T t_{ox}^2} D I_{SET} \quad (59)$$

where T is the temperature of the CF, t_{ox} is the dielectric thickness, k_B is the Boltzmann constant, D is the diffusion constant of the atomic species responsible for the generation of CF, I_{SET} is the current level at the onset of the transition, and $f_1 = n_e \lambda_e \sigma_e$, with n_e being the electron density, λ_e the electron mean free path and σ_e the cross-section for the electron-atom collision (responsible for the momentum transfer). V is the applied voltage across the BD spot which has been assumed to be equal to the overall externally applied bias between the metal contacts of the stack. f_1 value is around the unity since the defect concentration in the CF is most likely very high [172]. According to Equation (59), dI_T/dt is proportional to $D \times I_{SET}$. This means that the BD growth rate rises either by increasing the dominant diffusivity D of the fastest atomic species or by increasing the charge carrier flux.

The I - V characteristics under the PBD regime can be explained by some well-known physical models, for example invoking trap-assisted tunneling (TAT) current [187], cotunneling [188,189], and the quantum point contact model [159]. Although the transport properties of stacks with different materials are fitted by considering different transport models, the underlying concept is similar in all cases, the electrons passing through the PBD spots experience a very large energy loss. To simplify the approach, the BD spot I_{SET} - V curve is usually modeled by assuming a simple analytical dependence as described in [190].

It is important to mention that independent experiments have probed that power dissipation taking place inside the dielectric layer is a reasonable assumption. According to Takagi [191], electrons tunneling through defects responsible for stress induced leakage current (SILC) in thin oxynitrides loose a fraction of energy, and as shown by Blochl and Stathis [192], this is caused by defect relaxation. It is reasonable to assume that a

similar effect takes place for electron transport through the BD spot, since there is a clear dependence of the CF characteristic on the maximum current flowing through the device, both for the BD of gate oxides [179] and the SET event in RRAM devices [18,163,193], as well as for layered dielectrics, such as h-BN [168,190].

A simplification of spherical symmetry around the CF can be assumed to model the temperature in the BD spot. Within this approach, the temperature can be described by Equation (60), where the dissipated power at the CF is proportional to $I_{SET} \times V$, k_{th} is the thermal conductivity of the dielectric, T_0 is the room temperature and f_2 is the fraction of the energy lost at the constriction:

$$T = \frac{f_2 V I_{BD}}{2 \pi t_{ox} k_{th}} + T_0 \quad (60)$$

The fitting parameters are f_1 , f_2 , D_0 , and E_{act} ; (taking into consideration that $D = D_0 \cdot \exp(-E_{act}/k_B T)$) and they describe the main features of the progressive BD effect on different stacks [190].

In this section we considered a RRAM device based on a MIM stack with a 10 nm thick atomic layer deposited HfO₂ film sandwiched between Ti and TiN electrodes [193]. During the HRS to LRS transition the current (I_{Ti}) increases gradually with time evidencing the progressive nature of the SET event (see Figure 30a,b). It is a noisy and progressive process well in agreement with the literature [176–178,194] whose duration shows a strong voltage dependence and dispersion. The time evolution of the HRS to LRS transition is quantified by the slope dI_{Ti}/dt , as defined in [169,185,195]. TR values were experimentally evaluated through measurements such as those shown in Figure 30a,b (approximately 100 measurements for each voltage value).

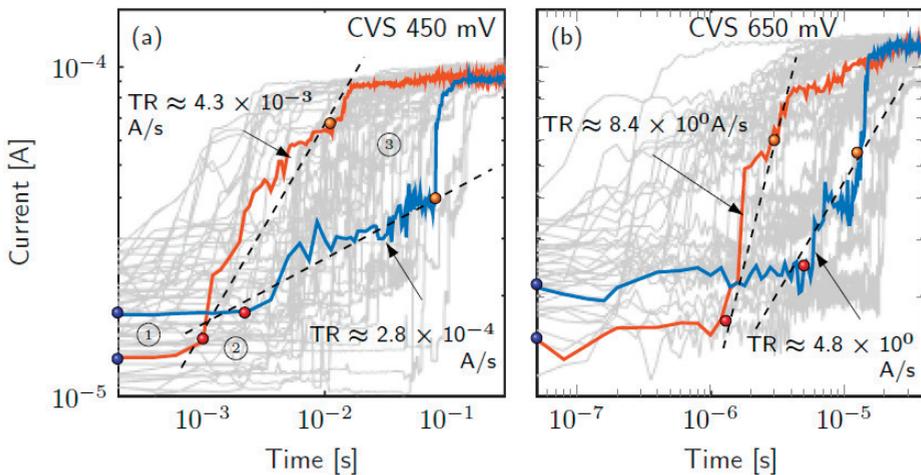


Figure 30. Current transient of the DUTs under constant voltage stress (CVS). (a) represents the lowest –450 mV– voltage whereas (b) the highest –650 mV–. Ball marker 1 points out the initial current (I_{init}), whereas 2 the onset of the progressive increase of current (I_{on}) and 3 the final jump to the compliance level (I_{end}).

The fitting results for TR as a function of the applied voltage, obtained with the proposed model in Equations (59) and (60), are illustrated in Figure 31. The proposed fit accounts for both the t_{ox} reduction (t_{ox} considered is equal to $t_{gap} \sim 2$ nm due to the forming step) and the increase in diffusivity (D_0 is in the order of $\sim 10^{-6}$ cm²/sec as other species are considered to complete the CF, i.e., oxygen vacancies). The rest of the parameters involved remain as previously mentioned in the literature ($E_{act} \sim 0.3\text{--}0.7$ eV, $f_2 \sim 0.1$ and $f_1 \sim 1$) [193].

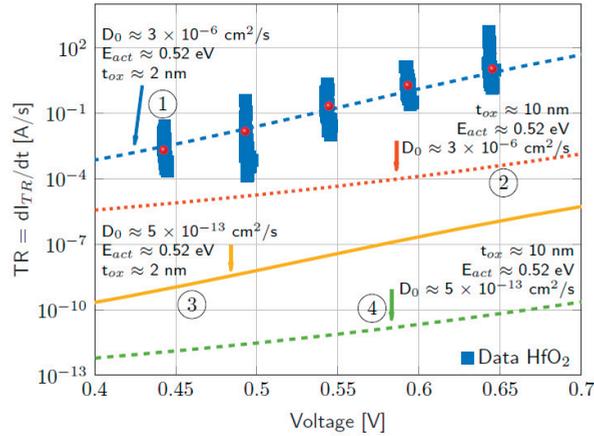


Figure 31. TR data (square markers –ball markers represent the mean value–) fitted assuming oxygen vacancies and $t_{gap} = t_{ox}$ (cyan dashed line – curve N° 1). Additionally, TR assuming literature values for t_{ox} and D is plotted –curves N° 2, 3 and 4–. TR presents a strong dependence with applied voltage, increasing almost one order of magnitude for every 50 mV step.

To implement this model for the SET event, the effect of the t_{ox} reduction after the forming step was considered. First, a forming operation (a controlled dielectric BD) creates the CF through the fresh oxide layer. Then, the switching mechanism is driven by the creation of a gap (RESET) and the restoration of the CF (SET). In the case under study, it has been demonstrated using the statistics of the SET switching time (t_{Set}) (i.e., the time to complete the HRS to LRS transition) that $t_{gap} \approx 2$ nm is a reasonable value [193].

Figure 32 presents the temperature calculations as a function of voltage provided Equation (60). f_2 represents the fraction of energy lost by the carriers, which ranges from 0 to 1. This parameter also depends on the temperature, mainly because of phonon-electron scattering [183]. Therefore, f_2 is a function of voltage and temperature whose behavior is found by a best fitting procedure. The influence of f_2 on the temperature is shown in Figure 32 for different f_2 values.

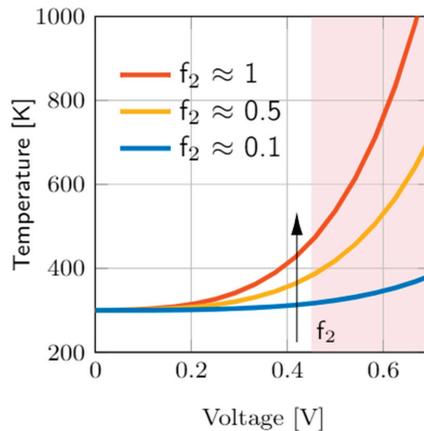


Figure 32. Temperature estimation according to Equation (60) as function of voltage and the energy loss in the CF. The red shaded zone indicates the voltages employed for the CVS (0.45 to 0.65 V).

The best fitting diffusivity required to reproduce the TR vs. voltage is observed in Figure 33. The data have been calculated assuming that D_0 is in the order of $3 \times 10^{-6} \text{ cm}^2/\text{s}$ and $E_{act} = 0.52 \text{ eV}$ as indicated in [193]. In HfO_2 -based RRAM devices, the SET event is explained as the completion of the gap due to the migration of O_2 -ions through a field-assisted and thermally activated effect, which creates the oxygen vacancies that fill the gap along the CF [38,44,53,195,196]. This is quite a relevant point to notice, as the diffusivity of oxygen vacancies (OVs), in a HfO_2 layer of thickness like t_{gap} spread over a range similar to the fitted diffusivity for the TR [197] (see Figure 33).

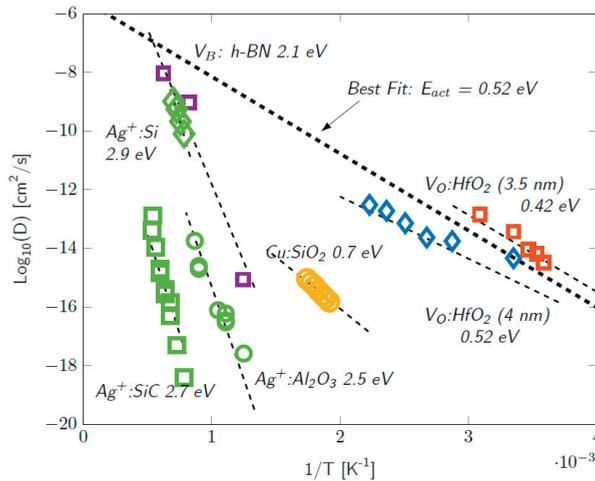


Figure 33. Reported values of diffusivity for different atomic species vs. reciprocal of temperature. The diffusivity D required for TR fitting is shown to be in the same range as the OVs diffusivity. OVs diffusivity [197] is $\sim 10^4$ times higher than for the metallic species as $\text{Cu}:\text{SiO}_2$ [198], $\text{Ag}:\text{SiC}$, $\text{Ag}:\text{Si}$ and $\text{Ag}:\text{Al}_2\text{O}_3$ [199,200]. VB diffusivity in h-BN data corresponds to [201].

The diffusivity required to fit the experimental data of catastrophic BD in both SiO_2 and high- k (Al_2O_3 or HfO_2) stacks with metal electrodes are of the order of $10^{-13} \text{ cm}^2/\text{s}$ at 1000 K, with activation energies ranging from 0.3 to 0.7 eV [169], where such values are in a range compatible with the diffusivity of metals in dielectrics (see in Figure 33. the case of Cu diffusion into SiO_2 layers [198]).

It should be mentioned that the state transition for a non-volatile regime in metal/h-BN/metal stacks (i.e., non-reversible event) has been studied with a similar approach where the best fitting value E_{act} is also much larger ($E_{act} = 1.3 \text{ eV}$) [184,189]. Such discrepancies may lay on the fact that the particular species involved in the electromigration and/or diffusion process may change, depending on the severity of the SET event (volatile and non-volatile), as it occurs between the BD and SET events in HfO_2 stacks. While in the BD event in HfO_2 the diffusing ion species are considered to be the metallic ions from the electrodes ($D_0 = 1 \times 10^{-13} \text{ cm}^2/\text{sec}$, $E_{act} = 0.3\text{--}0.7 \text{ eV}$ [159,169,189]), the migration of oxygen vacancies from the TMO layer are responsible of the SET transition event ($D_0 = 1 \times 10^{-6} \text{ cm}^2/\text{s}$, $E_{act} = 0.52 \text{ eV}$) [188].

To make clear the impact of both the t_{ox} reduction and the diffusivity increase (D_0), alternative fitting values were used to plot curves N° 2, N° 3 and N° 4 in Figure 31. Curve N°4 coincides with the TR for gate-oxide BD, as it considers diffusivity of metals in oxide layers and no t_{ox} reduction. The comparison of curves N° 1 and N° 4 evidence that TR is significantly higher than the TR expected for the voltage range considered. It is important to point out that TR calculated considering only a t_{ox} reduction or an increase in diffusivity (D_0) cannot meet the experimental data. This can be interpreted as that the two factors

determine the dependence with the TR voltage, since none of them can separately adjust the results independently.

6. Conclusions

A comprehensive and exhaustive revision of RRAM thermal models is presented. Different approaches have been considered and described, including different conductive filament geometries, operation regimes, filament lateral heat losses, several temperatures to characterize each conductive filament, etc. A 3D numerical solution of the heat equation within a RRAM simulator was used. In addition, analytical models have been developed using equations describing the relevant physics behind the heat equation accounting for steady-state and non-steady-state device operation. A general memristor modeling framework was formulated considering the temperature as a state variable. Moreover, the quantum perspective was included in a mesoscopic context; this is a must due to the nanometric dimensions of the devices under study. In this respect, thermal effects were considered in the formulation of the quantum point contact model. Finally, conductive filament thermometry in usual RRAM technology was studied in detail. Since the physics underlying resistive switching is mainly based on thermally activated physical mechanisms, an accurate description of thermal effects is essential. As far as we know, there are not similar manuscripts that put together these types of effects under one roof.

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Article

Characterization and Design of Photovoltaic Solar Cells That Absorb Ultraviolet, Visible and Infrared Light

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Abstract: The world is witnessing a tide of change in the photovoltaic industry like never before; we are far from the solar cells of ten years ago that only had 15–18% efficiency. More and more, multi-junction technologies seem to be the future for photovoltaics, with these technologies already hitting the mark of 30% under 1-sun. This work focuses especially on a state-of-the-art triple-junction solar cell, the GaInP/GaInAs/Ge lattice-matched, that is currently being used in most satellites and concentrator photovoltaic systems. The three subcells are first analyzed individually and then the whole cell is put together and simulated. The typical figures-of-merit are extracted; all the $I-V$ curves obtained are presented, along with the external quantum efficiencies. A study on how temperature affects the cell was done, given its relevance when talking about space applications. An overall optimization of the cell is also elaborated; the cell's thickness and doping are changed so that maximum efficiency can be reached. For a better understanding of how varying both these properties affect efficiency, graphic 3D plots were computed based on the obtained results. Considering this optimization, an improvement of 0.2343% on the cell's efficiency is obtained.

Keywords: concentrator systems; GaInP/GaInAs/Ge; multi-junction; photovoltaics; solar cells; space; triple-junction

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1. Introduction

The constant search for new energetic solutions to face the ever-demanding world's energy consumption has been one of the main focus amongst researchers in the twenty-first century. At the time this article is being written, a good and affordable alternative seems to be found in the use of renewable energies [1–19]. Even though the world is not yet prepared to switch completely to renewable sources, the installed capacity of these sources is increasing day by day, with the global renewable generation power already surpassing 2300 gigawatts. In 2018, 20% of this total generation capacity came from solar power, that continued to dominate in terms of new power installed, representing an increase of 24% [1].

This global solar expansion mainly derives from the capability of the photovoltaic (PV) industry to face the challenges that have been proposed until now.

In the years to come, PV has the capacity of becoming one of the major energy sources in the world—as the price of fossil fuels continuously rises [6–19], the cost of solar PV has been substantially decreasing over the last two decades, with its LCOE (Levelized Cost Of Energy) being estimated to be within the range of 0.03 to 0.10 \$/kWh by 2020–2022 [2,3,20]. This prophesizes a solid future for the PV industry, especially if it is supported by the decrease in battery prices.

All of this motivates the industry to come up with new and improved solutions; one of those improvements in recent decades is the use of III-V multi-junction solar cells. These photovoltaic devices employ III-V semiconductors (made of elements in groups III and V

of the Periodic Table), typically in a stacked distribution [4,5,21,22]. These cells have been demonstrating solid results in terms of efficiency, since the first III-V GaInP/GaAs tandem cell was demonstrated by Olson and Kurtz at NREL in 1996, with a record efficiency of more than 30% [21]. Today, III-V cells already hit the mark of 45.7% in concentrator photovoltaics (NREL, 4-junction GaInP/GaAs/GaInAs/GaInAs, 234 suns) [22], demonstrating extraordinary advances in choosing optimal bandgap distributions.

This work will focus on a specific III-V cell, the GaInP/GaInAs/Ge lattice-matched cell, the state-of-the-art cell for both concentrator photovoltaics and space applications. The main objective is then to build a simulation model that allows for a characterization of the subcells that form the whole cell, extracting $I - V$ curves and external quantum efficiencies, along with the most relevant figures-of-merit, such as fill-factors and efficiencies. A general optimization of the cell will also be attempted; this will be done by altering the thickness and doping of some layers.

It is used a Finite Element Tool, for being capable of simulating a 2D and 3D solar devices by providing a large set of physical models (drift-diffusion, general optoelectronic interactions with ray tracing, Fermi-Dirac statistics, etc.) for semiconductor device simulation.

2. Fields of Application of III-V Solar Cells

The III-V MJ (multi-junction) solar cells are utilized in the most varied fields of application, the most important two being space applications and concentrator photovoltaic (CPV) systems, as illustrated respectively in Figure 1a,b. These two fields represent very different operating conditions for solar cells, and thus different design approaches for each field must be considered. Record efficiencies of 35.8% (AM0 spectrum) [23] and 46% (AM1.5d spectrum, 508 suns) [22] were already demonstrated for space and CPV applications, respectively.



Figure 1. Some examples of solar cells use in space and terrestrial applications: (a) NASA's InSight Lander robot, powered by solar energy, and already owns the off-world record of power generation. (b) A HCPV parabolic system that uses high-efficiency multi-junction modules by Solartron Energy Systems.

2.1. Space Applications

Regarding space applications, III-V cells have become the go-to technology, not only because of their high-efficiency results but also because of their high tolerance to radiation exposure. After being irradiated with high radiation doses, these cells showed an EOL (end-of-life) efficiency that was higher than a BOL (beginning-of-life) efficiency of a standard Si solar cell. Of course, this represented a major change for the spacecraft industry, since a good EOL efficiency is intrinsically connected to the weight and cost of the overall system, paramount factors when discussing the launch of a spacecraft, in which the cost is determined by $\text{€}/\text{kg}$, as opposed to $\text{€}/W_p$ in terrestrial applications.

Therefore, these cells, given their high EOL efficiencies, good radiation tolerance, and high power-to-mass ratios (W/kg), meet the requirements of the majority of the NASA OSS (National Aeronautics and Space Administration Operational Support Services) missions, that call for high specific power values, making them the state-of-the-art cells for the majority of satellites and space vehicles.

Another important aspect concerning missions in space is the temperature at which PV modules must operate in certain harsher environments. Space PV arrays must be prepared to endure both high and low temperatures, depending on the mission's orbit. This leads to the necessity of studying the cell's temperature coefficient ($d\eta/dT$) to have a measure on how the performance of the cell will vary with temperature. When under the AM0 spectrum, the normalized temperature coefficient of a Si solar cell is in the range of $-3 \times 10^{-3} / ^\circ\text{C}$ to $-5 \times 10^{-3} / ^\circ\text{C}$, while for tandem GaAs/Ge cells the temperature coefficient is approximately $-2 \times 10^{-3} / ^\circ\text{C}$ [24].

This notorious difference in temperature coefficients is explained by the variance of bandgap in both cells; solar cells that have in their composition materials with higher bandgap values show lower efficiency losses with temperature [25]. This means that there will be an ideal bandgap for each operating temperature.

2.2. Terrestrial Concentrator Systems

On Earth, the task of implementing III-V plate modules would represent a heavy cost of production, with the cost of a typical III-V high-efficiency cell being around 10 \$/cm² [26]. To counter this problem, solar PV companies developed concentrator photovoltaic systems (CPV), in which sunlight is concentrated with the use of mirror lenses. Usual concentration ratios for III-V cells may go from 500× to 2000×, the latter being commonly called high concentration PV (HCPV).

The increase in irradiance will directly affect the short-circuit current of the cell, increasing it. Resorting to Equation (1), it is easy to see that incrementing I_{SC} affects the open-circuit voltage of the cell, which increases logarithmically by several KT/q factors. This boost in the V_{OC} will be more evident for a multi-junction cell, in which every subcell will contribute for the increase of V_{OC} with concentration, and thus rising the fill-factor of the overall cell [6–19].

$$V_{OC} = nV_T \ln \frac{I_{SC}}{I_0} + 1 \quad (1)$$

For this reason, it would be fair to think the higher the concentration ratio, the higher the efficiency of the cell. Alas, in reality, no device is ideal, including solar cells; there are always losses that need to be considered, such as series and shunt resistances that must be taken into consideration. The concentration increase will have a dominant impact on the overall efficiency, diminishing the FF (Fill Factor), and changing the $I - V$ characteristic. The greater the concentration ratio, the higher the impact will be on the cell; e.g., for the TJ (triple-junction) GaInP/GaInAs/Ge, when incrementing the series resistance from $R_s = 0$ to $R_s = 0.1 \Omega$, the FF is reduced from 90% (1 sun) to 87% at 83 suns, and to 71% at 500 suns [27].

Analyzing this data, it was then evident that some changes in series and shunt resistances had to be made in such a way that cells could operate under high concentration levels so that losses could be, to an extent, negligible. Every concentrator cell has a concentration limit for which the efficiency will start to drop, and several studies are being conducted in this matter. In the work of Steiner et al. [28], three tests were made using the single junction GaAs solar cell to prove the reduction in the FF and efficiency: three optimized grids for concentrations of $C = 100$, $C = 450$, and $C = 1000$ were tested, and the cell showed a maximum efficiency of 29.09% for a concentration of 450 suns.

3. III-V Solar Cell Design

For a better understanding of the fundamentals behind a III-V solar cell it is necessary to perceive where they differ from the simple junction cell. It has already been stated that III-V multi-junction cells are top performers in their fields of application, when compared with their single-junction counterparts, given that the latter have their efficiency limited a priori.

3.1. Bandgap versus Efficiency

In order to grasp why single-junction cells are limited efficiency-wise, one has to fathom how the bandgap is of paramount importance when discussing solar cells.

Taking into consideration a single-junction solar cell with bandgap W_G , only photons with their energy higher or equal to W_G are absorbed. Photons for which the energy is higher than the bandgap W_G , there is a certain amount of energy that is in excess and will be lost, a phenomenon also known as thermalization losses. This means that the energy that will be effectively converted into electric current will be just a portion of the photon's total energy. With this, it is evident that the device will only operate at maximum efficiency when the photon's energy, W_{ph} , is equal to the bandgap W_G . Alas, when considering the wide spectrum of sunlight, absorbing just the photons of a specific wavelength imposes quite a limitation on the overall efficiency of the cell.

In trying to solve this problem, a few solutions were developed. One of them is broadly used today in the PV industry: the concept of multi-junction solar cells. Instead of trying to make the cell operate only at a specific wavelength, one could try to divide the light spectrum into several spectral sections and associate a subcell with an appropriate bandgap to each one of them. This way, every subcell would have the unique function of absorbing photons of a specific wavelength range.

Now, there are different approaches to solve the problem and split the sunlight's spectrum. The first is a quite intuitive one, called the spatial distribution method, illustrated on Figure 2a, and consists in using a prism to separate a beam of white light into several different wavelengths and spatially arranging subcells with different bandgap values accordingly.

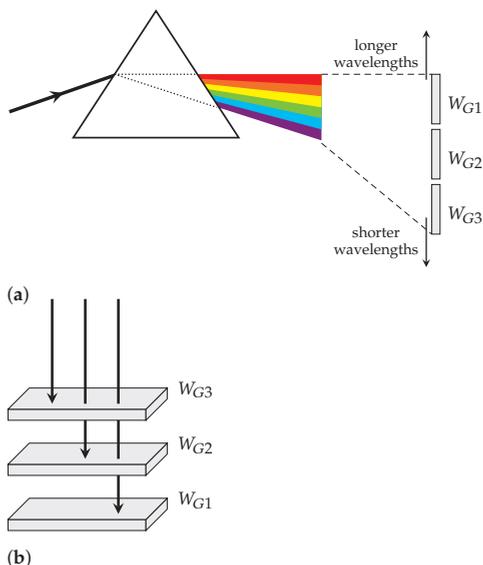


Figure 2. Spectral splitting approaches: (a) Spatial distribution, with the use of a prism, and (b) Stacked distribution of a 3-junction cell.

Even though the spatial distribution is employed in some CPV (concentrator photovoltaic) systems, there are some difficulties associated when using this method. The approach that is broadly used nowadays when designing MJ solar cells is the stacked distribution, as presented in Figure 2b. This method consists in stacking the subcells on top of each other by order of bandgap, so the subcell with a lower bandgap is placed on the bottom of the cell and the one with a higher bandgap is placed on the top. This way, the high energy photons can be absorbed right on top of the cell by subcells with high bandgap values,

forcing the low energy photons to penetrate further into the lower layers, where the low bandgap subcells are placed. As a result, the photons will be efficiently distributed and absorbed throughout the stack, increasing overall performance.

For this reason, the choice of bandgap combinations is a decisive step in multi-junction design. Given that III-V semiconductors show high versatility in possible bandgap combinations, they are one of the best choices for designing state-of-the-art solar cells. Bearing this in mind, Fraunhofer ISE developed the etaOpt software, capable of predicting cell efficiencies based on how many p–n junctions they are made of and what are their respective bandgaps. According to the results obtained from etaOpt, the efficiency can increase substantially with the number of p–n junctions, however, this gain is dampened for higher counts, i.e., a jump from 2 to 3 junctions provides a much larger increase than one from 5 to 6 junctions [29]. Knowing this data *a priori* is quite important for manufacturers, since the amount of efficiency gained may not justify higher production costs that derive from augmenting the number of p–n junctions.

3.2. Bandgap versus Lattice Constant

The choice of an appropriate bandgap does not take into account only the spectral regions, but also the choice of the lattice constant, since one depends on the other. This selection determines the structure of a MJ solar cell—if the materials all have, approximately, the same lattice constant, the cell is said to be lattice-matched; on the contrary, when the materials have different lattice constants, one says that the cell is lattice-mismatched or metamorphic (MM).

This distinction is significant when discussing solar cell design, given that stacked materials with different lattice constants may create dislocations, which can ruin the quality of the material and thus its performance. The production of metamorphic cells has to consider appropriate strategies, such as step-graded buffers that make the transition between two materials with different lattice-constants less abrupt.

4. The GaInP/GaInAs/Ge Solar Cell

Regarding this work, it seems only relevant to discuss approaches in which the GaInP/GaInAs/Ge solar cells are utilized. The two most relevant examples are the lattice-matched triple-junction and the upright metamorphic structures [4,5].

4.1. III-V Solar Cell Designs

At the time this article is being written, the lattice-matched triple-junction $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}/\text{Ga}_{0.99}\text{In}_{0.01}\text{As}/\text{Ge}$, on Figure 3a, is the state-of-the-art cell for both space and terrestrial concentrator applications. The subcells are all lattice-matched to Ge, assuring that no dislocations are created. The cell itself consists of three main p–n junctions composed of GaInP, GaInAs, and Ge, stacked on top of each other, connected in series. The light falls on the GaInP subcell, which has the higher bandgap, as it was already explained previously. Each one of these subcells is connected through tunnel junctions with low resistance and high optical transmissivity coefficients. However, one of the problems of this approach is that the spectrum splitting is not optimal, resulting in an excessive current in the bottom Ge cell.

One possible way to counter this problem is to increase the absorption of photons in the upper cells, resulting in less current discrepancy. This can be achieved by lowering the bandgaps of the top and middle subcells by increasing the In composition in both $\text{Ga}_x\text{In}_{1-x}\text{P}$ and $\text{Ga}_x\text{In}_{1-x}\text{As}$ materials. By doing this, the lattice constant also alters, and thus the materials no longer have the same lattice constant, making the cell lattice-mismatched or metamorphic (MM). This type of approach in monolithic structures may derive in dislocations that can harm material quality if no special measures are taken. In the case of the upright metamorphic TJ GaInP/GaInAs/Ge cell, presented in Figure 3b, one of those measures is to implement a GaInAs graded buffer between the middle and bottom cells, so that the lattice constant increases gradually and not abruptly.

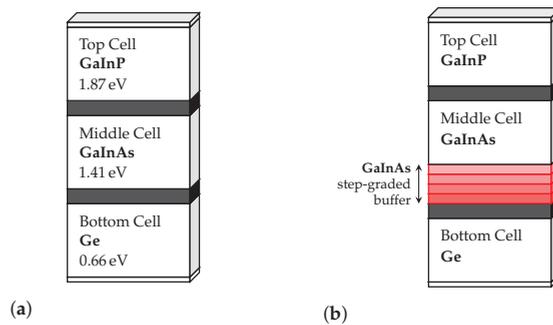


Figure 3. Simplified schematic of the triple-junction $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}/\text{Ga}_{0.99}\text{In}_{0.01}\text{As}/\text{Ge}$ cell: (a) lattice-matched, and (b) upright metamorphic approaches.

4.2. Simulating the LM State-Of-The-Art Cell

In order to simulate this cell, one has to take into account that several companies are currently researching various approaches to its development, the two most important being Fraunhofer ISE and Spectrolab, Inc.

In this work, the approach that was utilized is identical to the one used at Spectrolab, where this cell already demonstrated an efficiency of 32% under 1-sun (AM1.5G spectrum) [30]. Moreover, it is assumed a 1 cm^2 active area. While there is published research of this cell concerning some of its specific structural information, there are not many details available about doping and thickness values and the material compositions of each layer, given that all of these specifics are treated as proprietary information of Spectrolab.

Having as basis the detailed Ph.D. dissertation of Sharma [31], it was possible to put together an accurate model to simulate the cell. Some modifications were made to best adapt the cell to the one demonstrated by Spectrolab in the research paper of King et al. [30]. The simulated cell structure with all its layers is illustrated in Figure 4.

Firstly, to comprehend how the stacked cell works, it is necessary to perceive the role that each subcell plays in the monolithic cell by analyzing the materials that constitute each layer.

4.2.1. The GaInP Top Subcell

Beginning from top to bottom, the first step was to simulate the GaInP top cell. This cell, as stated previously, has to absorb high energy photons, since it is on top of this cell that the light beams will fall onto. The $\text{Ga}_x\text{In}_{1-x}\text{P}$ material is then chosen for its bandgap, which is $W_G = 1.89\text{ eV}$ for a composition of $x = 0.5$. This is a pretty high value that allows for the first high energy photons to be absorbed.

Besides the main p–n junction being composed of GaInP, the top subcell also contains two extra layers: the back-surface (BSF) and the window or front-surface (FSF) layers.

The window layer acts as an absorber layer, and thus it will have to have a high bandgap, small thickness, and a low series resistance. The material chosen can be the AlInP since it has a pretty high bandgap value and it is capable of being lattice-matched to the rest of the cell.

In contrast, the BSF layer exists to boost the short-circuit current of the cell, given that sharing the applied voltage across the n–p–p+ junctions minimizes the reflection of minority carriers and therefore leads to the decrease of the dark current. The material that is chosen for this is the quaternary AlGaInP.

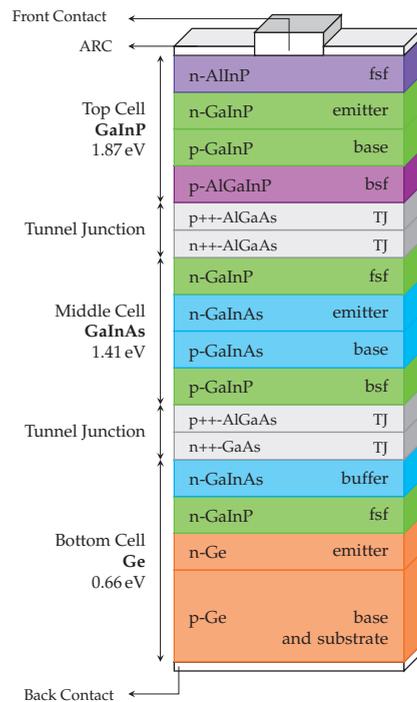


Figure 4. Detailed schematic of the simulated LM $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}/\text{Ga}_{0.99}\text{In}_{0.01}\text{As}/\text{Ge}$ solar cell.

4.2.2. The GaInAs Middle Subcell

The second subcell to be simulated is the middle GaInAs cell, which is based in the more simple GaAs solar cell. It is lattice-matched to all the components that form the whole monolithic cell, with the main ternary compound, $\text{Ga}_x\text{In}_{1-x}\text{As}$, having the composition $x = 0.99$ since its lattice constant corresponds to an exact-match to Ge's.

The subcell also has window and back-surface layers that are composed of highly-doped GaInP (composition of $x = 0.5$) given the high optical output of this material.

4.2.3. The Ge Bottom Subcell

Finally, the bottom subcell is made of a Ge substrate, instead of the typically used GaAs. This has two major advantages; firstly, Ge is cheaper than GaAs, and secondly, since Ge has a very low bandgap ($W_G = 0.66$ eV) the thickness of the subcell can be reduced from around $300\ \mu\text{m}$ for the GaAs substrate to $170\ \mu\text{m}$ for the Ge substrate.

Apart from a GaInP window layer similar to the middle cell one, the subcell also has a buffer layer made of highly-doped n-GaInAs (composition of $x = 0.99$) in order to reduce the ohmic contact between the bottom cell and the tunnel junction.

4.2.4. I–V Characteristic of the Stacked Cell

With the subcells already demonstrated, the next step was to try and assemble all of them in a monolithic cell.

Besides stacking the subcells on top of each other and separating them with appropriate tunnel junctions (AlGaAs–GaAs and AlGaAs–AlGaAs), it was also necessary to emulate the resistivity between subcell–tunnel diode and tunnel diode p–n junctions. This is made by establishing ohmic contacts with extremely high resistances that act as boundary conditions.

Two simulation models were tested: the first one, the cell was simulated in a Finite Element Tool without the metal grid (MG) on top, and the front contact had the same horizontal extension of the rest of the cell layers. This approach is a 1-D model since the structure only varies in one direction (vertical). The results were, then, artificially high since the contact effects were not being considered; the second method was employed so that the model would consider contact effects of the metal grid. Ergo, the cathode (top electrode) became smaller and a cap layer made of n+-GaAs was put below it with good ohmic contact formation in mind. Since there is this variation in the horizontal axis now, the model is a 2-D model.

Having as a reference the structure of the cell used at Spectrolab, the model developed in the Finite Element Tool was identical to the one depicted in Figure 4. In Figure 5, the obtained $I - V$ characteristics are presented for both simulation models: 1-D model (without the MG) and 2-D model (with the MG). The most important figures of merit obtained from the simulated results are shown in Table 1; for comparison purposes, the experimental results from Spectrolab, Inc. [30] are also presented.

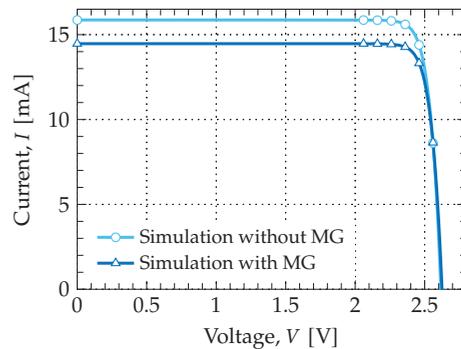


Figure 5. Simulated $I - V$ characteristics of the stacked cell. All curves were obtained using the AM0 spectrum. Figures of merit are presented in Table 1.

Table 1. Comparison of experimental and simulation values for the stacked cell.

	Experimental	Simulation	
	(Spectrolab)	without MG *	with MG *
I_{SC} [mA]	14.37	15.8771	14.4693
V_{OC} [V]	2.622	2.6296	2.6248
V_{MP} [V]	2.301	2.39	2.38
FF	0.85	0.89	0.88
Eff. [%]	32.0	36.9	33.65

* metal grid.

Analyzing the results, one can see that the best model to emulate the original cell's behavior is the 2-D model, in which some of the device's losses are being considered. The cell was emulated successfully to some extent: both the open-circuit voltage and short-circuit current were fairly replicated, which means that the overall structure (region materials, thickness, doping, etc.) was correctly modeled. Alas, both the fill-factor and efficiency were not consistent with the experimental results from Spectrolab. One explanation for this may be that losses were not properly accounted for in the final model, even taking the metal grid under consideration.

4.2.5. External Quantum Efficiencies

The final test was to obtain the External Quantum Efficiency (EQE) from each subcell when stacked. This analysis provides a frequency response of the cell, which can be precious information to understand and further optimize solar cells.

Resorting to the optical bias method, it was possible to extract the individual EQE of each subcell. This method consists of saturating all the subcells simultaneously, except the one under test, so that the saturated junctions will not limit the current, while that the cell that is not saturated (the one under study) will determine the current value, and thus its EQE can be computed.

When computing the EQE, it is necessary to have in mind that each cell will only absorb in a very specific wavelength range, that strongly depends on the bandgap of the other subcells. This dependence is due to the fact that the light spectrum is being split by the stacked distribution. In the lattice-matched approach, the GaInP top cell absorbs photons with energy $W_{ph} > 1.89$ eV, the GaInAs middle cell will absorb between the range of $1.89 > W_{ph} > 1.41$ eV and, finally, the Ge bottom cell will absorb photons with energy $1.41 > W_{ph} > 0.661$ eV. All of this is well illustrated in Figure 6, in which the simulated results in the Finite Element Tool are presented.

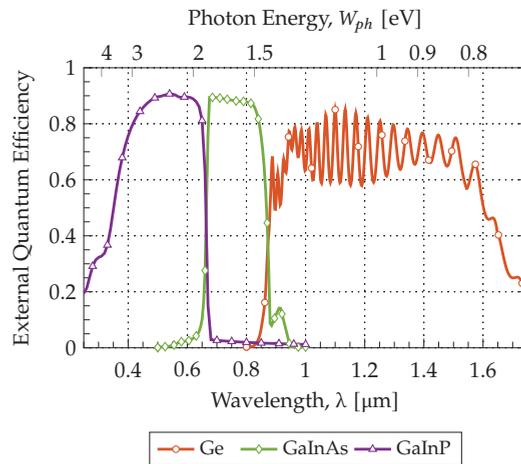


Figure 6. Simulated External Quantum Efficiencies of each subcell.

4.3. Temperature Effects

Temperature, naturally, is one of the most important factors when studying the behavior of semiconductors. This way, solar cells are usually tested for a nominal operating cell temperature (NOCT) of 25 °C, which is generally approximated to $T = 300$ K in absolute temperature values.

However, the photovoltaic cells under study have to be designed to withstand the extreme temperatures that only space can bestow. These temperatures can go from very high temperatures (HIHT (high intensity high temperature) missions) and deep-space temperatures like -170 °C, which is the cell temperature for Saturn-orbit missions. Therefore, it makes sense to try and emulate the cell under these conditions.

High and Low Temperatures

To try and perceive how high temperatures affect solar cell performance, a simulation was run first for $T = 300$ K and then for higher temperatures, in intervals of 50 K, to the final temperature of $T = 500$ K. Besides studying the cell's behavior at high temperatures, it is also important to understand how they perform at temperatures below 0 °C. Even if

some parameters variances can be expected, namely the increase in the open-circuit voltage and overall efficiency, there is some interest in how they vary for low temperatures.

The extracted $I - V$ curves for both ranges of temperature are illustrated in Figure 7, with the most relevant figures-of-merit from both plots (Figure 7a,b) being registered in Table 2.

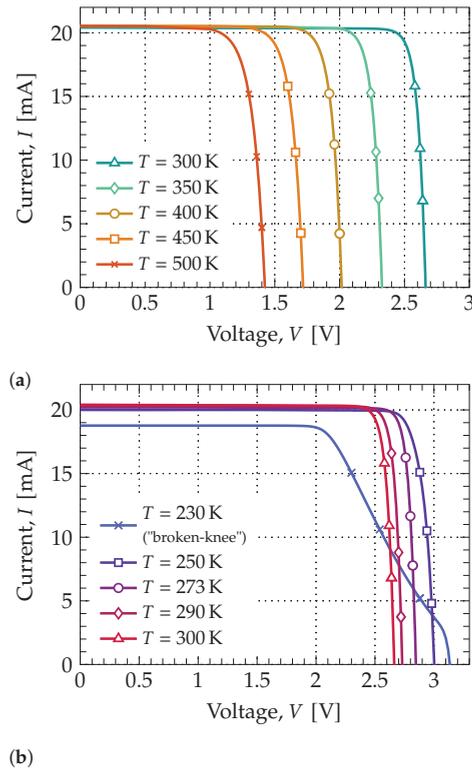


Figure 7. Tandem cell's $I - V$ characteristics obtained for two different intervals of temperature: (a) high temperature range, from $T = 300$ K to $T = 500$ K, and (b) low temperature range, from $T = 250$ K to $T = 300$ K. All curves were obtained using the AM0 spectrum.

Table 2. Measured values for both temperature ranges: high and low temperatures, from the respective plots (a) and (b), displayed in Figure 7.

	Figure 7a					Figure 7b			
	230 K	250 K	273 K	290 K	300 K	350 K	400 K	450 K	500 K
I_{SC} [mA]	18.7692	19.9959	20.2036	20.3397	20.4106	20.5206	20.5199	20.5445	20.5342
V_{OC} [V]	3.1344	3.0021	2.8466	2.7307	2.6627	2.3263	2.0162	1.7189	1.4237
FF	0.64	0.88	0.91	0.90	0.89	0.87	0.85	0.81	0.77
Eff. [%]	27.77	38.79	38.25	36.72	35.73	30.59	25.74	21.05	16.46

Both the open-circuit voltage and short-circuit current behave as expected: I_{SC} has an insignificant variance whereas the V_{OC} decreases substantially as temperature increases.

As for the efficiency and fill-factor, they both decrease as temperature rises, however, this is only valid to a certain point. As the array temperature gets colder, the variance in certain parameters begins to be non-linear. This is because, as temperature decreases, carriers start to enter the state of “freeze-out”, in which there is not enough thermal energy

for the dopants to be fully ionized, and thus there will be a shortage of charge carriers. Another issue is the phenomenon called “broken-knee” or “double-slope”, in which the $I - V$ characteristic becomes degraded, generating a great reduction in the fill-factor and efficiency—this can be seen in the obtained curve for $T = 230$ K.

Notwithstanding, colder environments, to a certain extent, are good for solar cells since there is a boost in the overall performance; the obtained results confirm the need for some PV panels to have cooling systems installed so that the power conversion efficiency is maximized.

5. Cell Optimization

With the lattice-matched GaInP/GaInAs/Ge solar cell properly reproduced and simulated, an overall optimization of the cell is attempted. In order to do this, two studies on how thickness and doping affect the overall performance of the cell were made. The first study takes into account the top and middle subcells and their respective thicknesses. The second study will take into account the doping of the GaInP top subcell. The properties of the whole cell were maintained constant with the default, previously simulated parameter values.

Considering that the cell that was being simulated up to this point was optimized for CPV (concentrator photovoltaic) applications, this work will attempt to perform an optimization for space applications in LEO (low-Earth orbit, <1000 km) missions. The spectrum utilized was the AM0 and the cell temperature was $T = 300$ K.

5.1. Thickness Variation

When varying the cell thickness, it is necessary to select which layers are going to be altered. Since the photocurrent of the entire cell is determined by the top cell, the first layers to be chosen were the GaInP- base and emitter layers. The BSF and FSF layers were not altered, since their values were already at the minimum possible. The main goal of this study is to choose thickness values that establish a compromise between efficiency and size of the cell, given that the less cell bulkiness the better.

The first test consisted in varying both base and emitter thicknesses of the top cell and evaluate the efficiency, η , improvement. Other parameters like short-circuit current, I_{SC} , open-circuit voltage, V_{OC} , fill-factor, FF , and the variation in efficiency, Δ_{Eff} , were also registered. Both default (gray) and best (green) obtained results for the first test are displayed in Table 3. The best efficiency achieved was 31.80% which in comparison to the initial value of 31.76% corresponds to an improvement of +0.1107%.

Table 3. First study, first test: Top GaInP subcell thickness variation of the p-base and n-emitter layers.

Base [μm]	Emit. [μm]	I_{SC} [mA]	V_{OC} [V]	FF	η [%]	Δ_{Eff} . [%]
0.75	0.10	18.6750	2.6251	0.8847	31.7687	0.0000
0.70	0.11	18.5956	2.6254	0.8893	31.8039	+0.1107
Default values ; Best obtained values						

The second test was analogous to the first, except it was made considering only the middle subcell thickness. Once again, the BSF and FSF layers were not altered, varying only the thickness of both GaInAs- base and emitter layers. The top GaInP layers' thicknesses were the initial ones, without employing the optimization of the first test. The default values along with the best-obtained results are presented in Table 4. Alas, in this case, the best-obtained results (in green) correspond to a thickness increase of $0.5 \mu\text{m}$ in the base thickness. Since a bulkier cell is not the desired outcome, the second-best results (red) that achieved an efficiency of 31.8036% were chosen. This efficiency value corresponds to an improvement of +0.1098%.

Table 4. First study, second test: Middle GaInAs subcell thickness variation of the p-base and n-emitter layers.

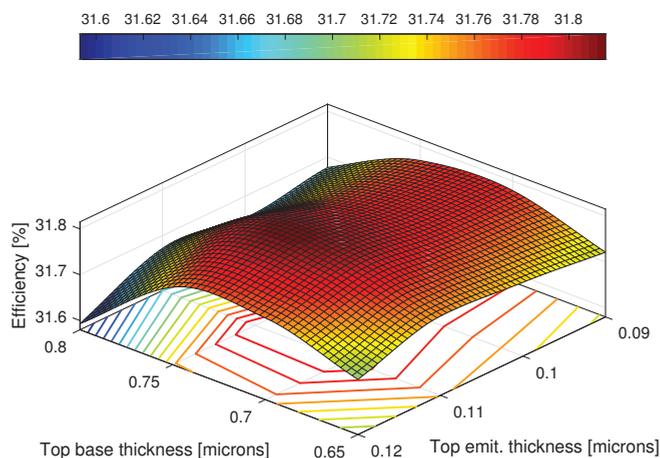
Base [μm]	Emit. [μm]	I_{SC} [mA]	V_{OC} [V]	FF	η [%]	$\Delta_{Eff.}$ [%]
3.50	0.08	18.6750	2.6251	0.8847	31.7687	0.0000
4.00	0.08	18.6744	2.6272	0.8851	31.8074	+0.1220
3.75	0.09	18.6861	2.6262	0.8847	31.8036	+0.1098
Default values ; Best obtained values ; Second best values .						

All of the obtained results for both tests are illustrated in two 3D plots, in which one can observe how cell the layers' thicknesses affect the overall performance of the cell. The 3D surface plots are presented in Figure 8 and were made resorting to the Curve Fitting Tool of MATLAB[®].

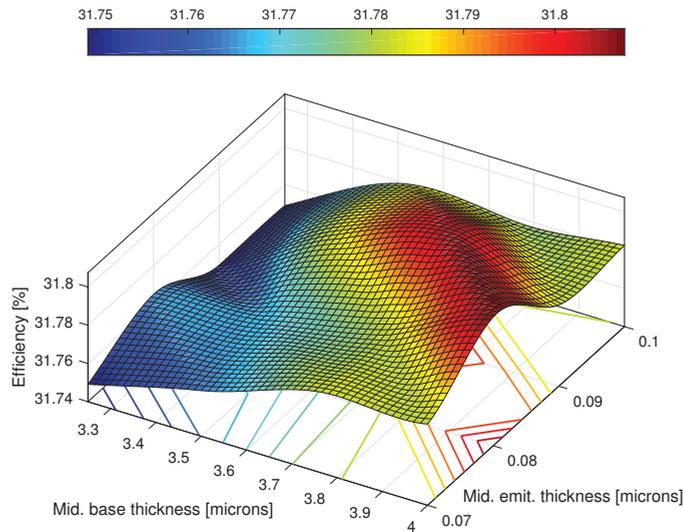
With this visual aid, it fairly clear that for the first test (Figure 8a), the efficiency depends on both GaInP- base and emitter thicknesses, being apparent that higher efficiencies concentrate in a range of values that are roughly in the center of the plot.

Similarly, analyzing the 3D plot for the second test (Figure 8b) it is evident that the higher the middle subcell's base thickness, the higher the efficiency. Unlike the first test, the GaInAs-base thickness is predominant in how the efficiency varies.

Finally, the best results from both tests were simulated, so that both subcell optimizations could be taken into account. The obtained parameters were: $I_{SC} = 18.5943$ mA, $V_{OC} = 2.6276$ V, $FF = 88.98\%$ and an efficiency of $\eta = 31.8431\%$, which translates in an improvement of 0.2343%, in comparison with the initial value.



(a)
Figure 8. Cont.



(b)

Figure 8. Graphic display of the obtained results for the: (a) first test: top GaInP subcell, and (b) middle GaInAs subcell. Both 3D plots were obtained using the 3D fitted surface with the cubic method of MATLAB Curve Fitting Toolbox.

5.2. Doping Variation

The second and final study was designed to evaluate how doping alters the performance of the cell. This last simulation is run with the best thickness values obtained in the first study.

Only the top cell’s base and emitter layers are going to be contemplated in this study. Once more, Table 5 shows the best-obtained results of doping variation for the GaInP- base and emitter layers. The best obtained efficiency was 33.0194%, which corresponds to a total improvement of +3.9368% of the very first efficiency value that was $\eta = 31.7687\%$ (refer to Tables 3 and 4).

Table 5. Second study: doping variation of the p-base and n-emitter layers in the top subcell.

Base [cm ⁻³]	Emit. [cm ⁻³]	I _{SC} [mA]	V _{OC} [V]	FF	η [%]	Δ _{Eff.} [%]
1 × 10 ¹⁸	1 × 10 ¹⁸	18.6371	2.6805	0.90	33.02	+3.9368
1 × 10 ¹⁷	5 × 10 ¹⁸	18.5943	2.6276	0.89	31.84	+0.2343
Default values ;		Best obtained values				

The doping values that were simulated were carefully chosen, given that the higher the doping, the lower the potential barrier to be overcome, making higher efficiencies possible to achieve. However, this efficiency increase can not be indefinite, since the minority carrier lifetime and diffusion length decrease with doping increase [32]. Hence, searching for the optimal doping value that increases efficiency without degrading the electronic properties of the semiconductor is of paramount importance. Values past $2.00 \times 10^{18} \text{ cm}^{-3}$ for the base and $1 \times 10^{19} \text{ cm}^{-3}$ were not chosen, given that simulations run with doping values higher than these resulted in deterioration of the *I* – *V* curve.

Analogously to the first study, a 3D fitted cubic surface of the results was plotted and it is illustrated in Figure 9. It is clear that the base doping is predominant in efficiency variation; as it increases, efficiency values increase, reaching a peak region in which the

efficiency is the highest possible. Beyond those values, there is an abrupt drop in the short-circuit current and open-circuit voltage, resulting in an efficiency reduction.

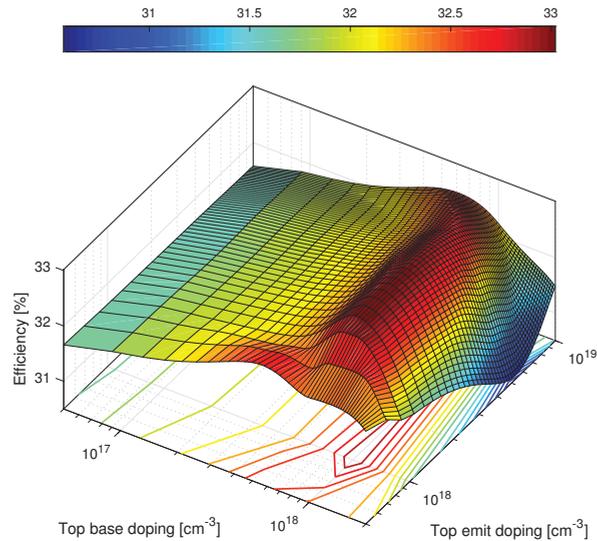


Figure 9. Graphic display of the obtained results of the second study. The 3D fitted surface with cubic method (MATLAB[®]).

This concludes the optimization of the cell for operation under the AM0 spectrum, at the nominal temperature of $T = 300$ K. As it has already been mentioned, temperatures in space can oscillate from extremely low to very high temperatures (sometimes in the same mission), and so each PV array must be optimized in accordance with the conditions it is planned to operate at.

6. Conclusions

The main aim of this work was to create a model so that a triple-junction state-of-the-art solar cell could be emulated and then analyzed with accuracy, without the need to resort to more advanced, and expensive, simulation technologies.

Comparing the simulated results with the actual experimental results by Spectrolab, Inc. one could say that the main goal was achieved, and the cell was emulated successfully. Both the open-circuit voltage and short-circuit current were fairly replicated, which means that the region materials, thickness, and doping were correctly modeled.

However, both the fill-factor and efficiency were not consistent with their experimental counterparts; this may have to do with the fact that losses were not properly accounted in the modeled cell since the only loss mechanisms present were the metal grid and the back/front contacts, and the fact that complex refractive indices were used in simulation (the imaginary part accounts for losses). Experimental values are calculated by appropriate measuring devices, such as multimeters, connecting them in series/parallel to a resistor, which in turn is connected to both terminals of the cell. This results in part of the losses not being accounted for in the simulation.

Other relevant differences are the external quantum efficiencies that were obtained for each subcell, in contrast with the experimental curves from Spectrolab, Inc. [33]. This is due mainly to the use of refractive indexes that do not correspond to the exact composition of a certain material. For instance, the most obvious difference is between the simulated and experimental frequency responses in the middle cell; this discrepancy may reside in the fact that the only refractive index available (from the databases) is not a rigorous match for

the composition of $x = 0.99$ in $\text{Ga}_{0.99}\text{In}_{0.01}\text{As}$. This explanation is valid for other ternaries used as well.

Furthermore, bearing in mind that temperature plays a significant part in semiconductor performance, a test to evaluate how temperature influences the cell was also conducted. Most of the published research on how the GaInP/GaInAs/Ge solar cell behaves under different temperatures only has into consideration the higher range of temperature, given its paramount use in concentrator photovoltaic systems. With spacecraft implementation in sight, it was thought to be relevant to verify how the cell behaviors at low temperatures. Even though some plausible results were obtained, simulations in temperatures below 230 K did not obtain convergence, considering that the cell's design was not prepared for such low-temperature environments.

Finally, an optimization of the GaInP/GaInAs/Ge LM cell was also conducted. In this optimization, certain cell parameters were tweaked so it could reach its maximum potential for a 1-AM0 incidence. This could prove of some value for the photovoltaic industry that is dedicated to the manufacturing of solar cells for space applications, given that the doping can significantly boost the cell's efficiency.

Regarding the simulation times, depending on the mesh fineness and the voltage step that are being employed, the whole model takes roughly six minutes to simulate with Newton's method. This may be an advantage over more complex and detailed ways of simulation that are more time-consuming if the main objective is simply to obtain the major figures-of-merit of the cell.

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Article

Optical Nanoantennas for Photovoltaic Applications

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Abstract: In the last decade, the development and progress of nanotechnology has enabled a better understanding of the light–matter interaction at the nanoscale. Its unique capability to fabricate new structures at atomic scale has already produced novel materials and devices with great potential applications in a wide range of fields. In this context, nanotechnology allows the development of models, such as nanometric optical antennas, with dimensions smaller than the wavelength of the incident electromagnetic wave. In this article, the behavior of optical aperture nanoantennas, a metal sheet with apertures of dimensions smaller than the wavelength, combined with photovoltaic solar panels is studied. This technique emerged as a potential renewable energy solution, by increasing the efficiency of solar cells, while reducing their manufacturing and electricity production costs. The objective of this article is to perform a performance analysis, using COMSOL Multiphysics software, with different materials and designs of nanoantennas and choosing the most suitable one for use on a solar photovoltaic panel.

Keywords: nanoantennas; optics; optoelectronic devices; photovoltaic technology; rectennas

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1. Introduction

In the last decade, the advances in the nanoscale dimension enabled the development of new devices, such as nanoantennas or optical antennas, due to the emergence of a new branch of science known as nanooptics, which studies the transmission and reception of optical signals at the nanoscale. These devices have been the object of intense research and development activity, with the goal to reach the captivating possibility of confining the electromagnetic radiation in spatial dimensions smaller than the wavelength of light.

The transmission through a metal plane with subwavelength-sized holes can be drastically increased if a periodic arrangement of holes is used. This phenomenon is widely known as Extraordinary Optical Transmission [1]. The usage of nanoantennas with apertures smaller than the light wavelength can locally enhance light–matter interaction. Thus, nanoantennas are devices that have the ability to manipulate and control optical radiation at subwavelength scales.

Nanoantennas are a nanoscale version of radio-frequency (RF) or microwave antennas. However, throughout this article it will be proven that in the process of sizing the nanoantennas, it will not be enough to reduce the size of the RF antennas to the optical domain, mainly because of the unique material properties of metals that influence the behavior of antennas at the nanoscale: the existence at the interface between metals and dielectrics of surface plasmon-polariton electromagnetic waves, which gives rise to resonant effects not available at RF [1,2].

The use of optical antennas for solar energy harvesting has received significant interest as they represent a viable alternative to the traditional energy harvesting technologies.

Economical large-scale fabrication of nanoantenna devices would support applications such as building integrated photovoltaics and supplementing the power grid [3].

2. Rectenna System for Solar Energy Harvesting

The nanoantenna itself does not convert the collected AC current into DC current, and so it needs to be complemented with a rectifying element. The whole structure is commonly referred to as a rectenna [4].

A rectenna is a circuit containing an optical antenna, filter circuits, and a rectifying diode or bridge rectifier for the conversion of electromagnetic energy propagating through space (solar energy) into DC electric power (through the photovoltaic effect).

A schematic representation of a nano-rectenna system is depicted in Figure 1.

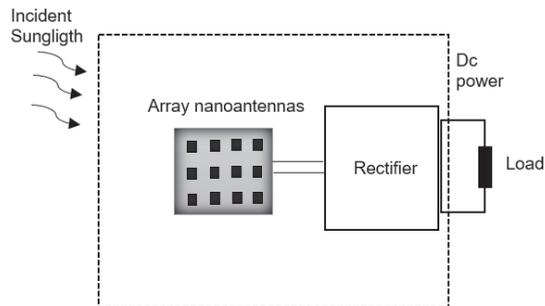


Figure 1. Representation of the nano-rectenna system (adapted from the work in [5]).

First, electromagnetic radiation is collected by the nanoantenna device. However, the output obtained from a single nanoantenna element is not enough to drive the rectifier and to provide DC power to an external load. The efficiency of a single optical antenna is generally low and its functionality is limited. Therefore, nanoantennas are arranged into arrays to increase their signal. The total field captured by the array is the addition of the fields captured by each nanoantenna [6].

The AC current generated in the nanoantenna arrays is collected and rectified into DC current by the rectifier system. This system has different rectifiers whose outputs can be DC coupled together, allowing arrays of nanoantennas to be networked to further increase output power [3].

As optical radiation requires high-speed rectification, high frequency metal–insulator–metal (MIM) diodes—also known as tunneling diodes—are commonly used for this purpose.

According to Moddel and Grover, the MIM diodes must have three key characteristics in order to have an efficient rectifier system [6]: high responsivity, that is, a measure of the rectified DC voltage or current as a function of the input radiant power; low resistance, in order to have a good impedance matching between the antenna and the diode; and asymmetry in the I–V curve, so the diode must have asymmetric characteristics for the rectenna be operated without applying an external DC bias.

Examples of material combinations used for diode rectifiers include Ni/NiO/Ni, Nb/Nb₂O₅/Pt, Nb/TiO₂/Pt, Cu/TiO₂/Pt, Nb/MgO/Pt, and Nb/Al₂O₃/Nb [6].

3. Experimentally Studied Nanoantenna Materials and Designs

A large variety of nanoantenna geometries has been researched for multiple potential applications. Currently, nanoantennas structures are mainly made of plasmonic materials, i.e., specially designed metal (usually gold or silver) nanoparticles with unique optical properties. Plasmonic materials exhibit strong light absorption in the visible region of the spectrum [4].

The advances in the manufacturing techniques allowed the construction of different formats of nanoantennas. The main types of plasmonic nanoantennas that have been proposed and investigated experimentally are represented in Figure 2.

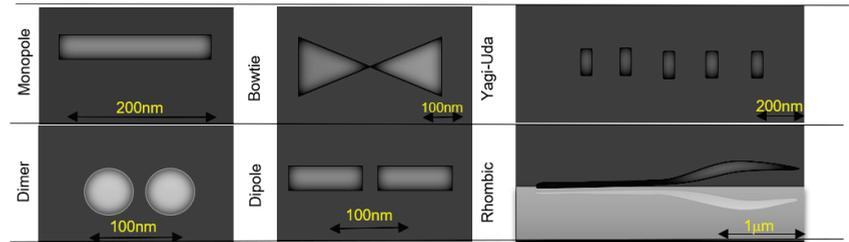


Figure 2. Main types of plasmonic nanoantennas (adapted from the work in [7]).

3.1. Plasmonic Monopole Nanoantenna

The most basic type of plasmonic nanoantenna, a monopole, is a single metallic nanoparticle that can enhance the electromagnetic field strength in its surrounding area upon excitation of plasmon resonances. Monopole nanoantennas have advantages over other geometries, because they are easier to engineer and are well isolated from interference due to the ground plane. Their characteristics are dependent on the shape, size, material, and dielectric environment of the nanoparticle [7].

Another great utility of the monopole optical antenna is when it is integrated in a Near-field Scanning Optical Microscopy (NSOM), to be used as a near-field probe for measurements [8]. An effective nanoantenna can be used in spectroscopy: it needs to interact strongly with incident electromagnetic radiation in order to measure its intensity.

3.2. Plasmonic Dipole Nanoantenna

Dipole configurations are widely used in radio frequency and microwave ranges. Therefore, it is not a surprise that analogs of such antennas also appeared in the optical range. This type of optical antenna is widely used in near-field optical probes, just like the monopole. The dipole optical antenna is constituted either by dimers or two monopoles separated by a small space (gap). Usually, there is a high field confinement in the gap between the two metallic nanoparticles [7].

The design of plasmonic nanoantennas may rely on the same principles used in RF antennas. For example, the length of the dipole RF antenna is approximately half the wavelength of the incident radio waves, whereas the length of the dipole plasmonic nanoantenna is smaller than the wavelength, λ , of incident light in free space [9].

3.3. Plasmonic Bowtie Nanoantenna

Another typical structure is the bowtie nanoantenna, consisting of two triangular shape nanoparticles aligned along their axes and forming the feed gap with their tips. These optical antennas are a variant of the dipole nanoantennas. Such geometry ensures a wider bandwidth together with large field localizations in the feed gap compared to the straight dipole.

The bowtie topology is considered to be one of the most efficient nanoantenna geometries for solar energy harvesting. According to Sen Yan [5], in their study it is shown that the bowtie topology can increase the total radiation efficiency and rectenna efficiency compared to the straight dipole by a considerable 10%.

3.4. Plasmonic Yagi-Uda Nanoantenna

RF Yagi-Uda type antennas are usually used to receive TV signals from remote stations, due to their high directivity. Their plasmonic counterparts consist of a reflector and one or several directors.

Yagi–Uda optical antennas can be useful in many applications: in wireless communications, in the fields of biology and medicine, in nanophotonic circuits, in quantum information technology, in data storage (as an optical chip), in photodetectors, and in photovoltaic (PV) systems.

3.5. Plasmonic Spiral-Square Nanoantenna

This design of nanoantenna allows the electromagnetic radiation to be harvested in one specific point in its structure—the gap (feed point) between two metallic arms, as presented on Figure 3. Thus, this topology has a wider angle of incidence exposure in comparison to other formats, which makes it an ideal geometry for solar energy harvesting.

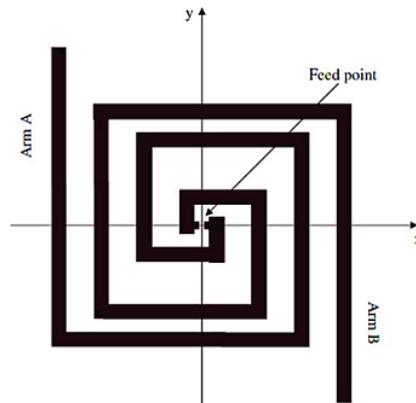


Figure 3. Geometry of a square-spiral nanoantenna (sourced from the work in [10]).

They also demonstrate a high directivity that can be further improved by increasing the number of arms.

3.6. Dielectric Nanoantennas

A new research direction of optical antennas has recently been suggested with the introduction of dielectric nanoantennas. Optical antennas constructed with dielectric materials have several advantages over their metallic counterparts due to unique features not found in plasmonic nanoantennas [4].

Dielectric nanoantennas are fabricated from optically transparent materials that have low dissipative losses at optical frequencies. Unlike gold or silver, dielectric nanoantennas are usually made from silicon nanoparticles which are widely used in nanoelectronics to fabricate transistors and diodes. Furthermore, silicon has a high permittivity and exhibits very strong electric and magnetic resonances at the nanoscale, and thus improves radiation efficiency and antenna directivity, expanding the range of applications for nanoantenna structures [4,11].

The authors of [11] used silicon nanoparticles to demonstrate the performance of all-dielectric nanoantennas. They have analyzed an all-dielectric analog of the plasmonic Yagi–Uda nanoantenna consisting of an array of nanoelements: four directors and one reflector particle made of silicon. In this type of structure, the optimal performance is obtained when the director nanoparticles sustain a magnetic resonance and the reflector nanoparticle sustains an electric resonance [4]. Schematic representation of this antenna is shown in Figure 4.

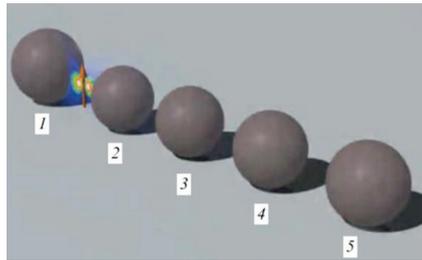


Figure 4. 3D view of an all-dielectric optical Yagi–Uda nanoantenna, consisting of the reflector 1 of the radius $R_r = 75$ nm, and smaller director 2–5 of the radii $R_d = 70$ nm (adapted from the work in [7]).

The dipole source is placed equally from the reflector and the first director surfaces at the distance D . The separation between surfaces of the neighboring directors is also equal to D .

The operational regime of a dielectric Yagi–Uda nanoantenna strongly depends on the distance between its elements. According to Krasnok [11], in their study it was verified that the radiation efficiency of the dielectric Yagi–Uda nanoantenna slowly decreased with decreasing distance between its elements, while the radiation efficiency of a plasmonic antenna of similar design and dimensions was greatly affected by the decrease in distance between particles. This is due to increased metal losses caused by proximity of adjacent metallic nanoparticles.

However, for larger separation distances, D , the radiation efficiencies of both types of nanoantennas were very identical. Although dissipation losses of silicon are much smaller than those of silver, the dielectric particle absorbs the EM energy by the whole spherical volume, while absorption only occurs at the surface of metallic particles. As a result, there is no substantial difference in the performance of these two types of nanoantennas for relatively large distances between its elements.

To sum up, based on the results of this study, a conclusion could be made that all-dielectric nanoantennas demonstrate major advantages over their metallic counterparts: much lower Joule losses and strong optically induced magnetization [11].

3.7. Aperture Nanoantennas

There is another type of optical antenna that is interesting for the topic of this article: aperture optical antennas. Light passing in a small aperture is the subject of intense scientific interest since the very first introduction of the concept of diffraction by Grimaldi in 1665 [12].

The first theory of diffraction due to a slit, that is much less than the light wavelength, in a thin metal layer was developed by Bethe. This theory predicted that the power transmitted by the slit would decrease as the slit diameter decreased relative to the wavelength of the EM radiation. This theory proved to be incorrect when Ebbesen, in 1998, observed the extraordinary optical transmission phenomenon (EOT) [1]. The EOT is an optical phenomenon, in which a structure containing subwavelength apertures transmits more light than might naively be expected. Ebbesen et al. observed that when focusing a light beam in a thick metallic film where there was a subwavelength hole array, a large increase of incident electromagnetic wave transmission occurs, i.e., a periodic array of subwavelength holes, as presented in Figure 5, transmits more light than a large macroscopic hole with the same area as the sum of all the small holes [1,2,13–19].

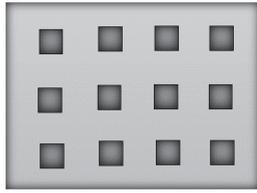


Figure 5. Schematic view of 200 nm diameter aperture arrays with 1 μm period (adapted from the work in [12]).

This discovery would be fundamental, as it not only allowed great technological developments during the last decade, but also allowed a better understanding of the diffraction by small slits in relation to the light wavelength [20,21].

According to Wenger, there are three main types of aperture antennas [12]: single subwavelength aperture, single aperture surrounded by shallow surface corrugations, and subwavelength aperture arrays.

4. Surface Plasmon Resonance

As referred in the introduction, incident light on the optical antenna causes the excitation of free electrons in metallic particles. More precisely, EM waves induce time-varying electric fields in the nanoantenna that apply a force on the gas of electrons inside the device, causing them to move back and forth at the same frequency range as the incoming light. This phenomenon is known as surface plasmon. At specific optical frequencies the nanoantenna resonates at the same frequency as the incoming light which enables the absorption of the incoming radiation [4,15–19].

It should be taken into account that, at optical frequencies, metals do not act as perfect conductors: their conductivity changes dramatically, and so they are unable to respond to the time-varying electric field immediately. The wave propagation within the material is affected, which means that the penetration of EM radiation into metals can no longer be neglected.

Thus, at optical frequencies an antenna no longer responds to external wavelength but to a shorter effective wavelength that depends on the material properties [20].

EM radiation penetrates the metal of the nanoantenna and gives rise to oscillations of the free-electron gas. These electron oscillations can give rise to plasmon resonances, depending on the size, shape, and index of refraction of the particle as well as the optical constants of its surrounding [21].

When these oscillations are optimized, i.e., when the metal structure is sized to achieve the resonance condition, it is called Surface Plasmon Resonance (SPR). It is also important to mention that there are two types of surface plasmons [15–19,22]: Surface Plasmon Polariton (SPP), when the EM waves strike a metallic film and are confined to the surface of this film, and Localized Surface Plasmon (LSP), when the coupling is made with a metal nanoparticle with a diameter much smaller than the incident wavelength.

Surface plasmons are highly confined energy fields made by the oscillation of electrons on the surface of nanoantennas. When a metallic nanoparticle is illuminated by light, surface plasmons will be coupled with the photons of incident light in the form of a propagating surface wave [23].

SPPs are infrared or visible frequency EM waves trapped at or guided along metal–dielectric interfaces [24]. This coupling of plasmons—either SPPs or LSPs—and photons results in charge oscillation in the visible and infrared regimes depending on the metal used. SPPs are shorter in wavelength than the incident light (photons). Therefore, SPPs provide a significant reduction in effective wavelength and have tighter spatial confinement and higher local field intensity [24].

Recent development of nanofabrication techniques enabled construction of a variety of metal structures at the subwavelength scale and opened the research area called plasmonics, a subfield of nanophotonics studying the manipulation of light coupled to electrons at the nanoscale.

The properties of optical antennas are still under the intensive study and so research efforts to relate plasmonics with subwavelength optical antenna are in a developing stage [23].

5. Efficiency

The radiation efficiency of nanoantennas is a key parameter for solar energy harvesting. It is the first factor in the total efficiency product by which nanoantennas can convert incident light to useful energy. This efficiency depends directly on the type of metal used as conductor and the dimensions of the nanoantenna [6].

The main advantage of this type of technology in comparison to the conventional solar photovoltaic cells is its far greater efficiency by which the transformation of electromagnetic energy into DC electric power is performed. Typical efficiencies for traditional silicon cells are in the order of 20%, whereas nanoantennas go from a stunning 70% for silver nanodipoles [25] to a more realistic 50% for aluminum dipoles [26]. Most solar radiation is in the visible and infrared (IR) wavelength region, and so nanoantennas need to be designed for this part of the spectrum, with the aim of being an alternative to conventional solar photovoltaic cells.

The total efficiency of a rectenna consists of two parts: (1) the efficiency by which the light is captured by the nanoantenna and brought to its terminals, also known as radiation efficiency, η_{total}^{rad} , and (2) the efficiency by which the captured light is transformed into low frequency electrical power by the rectifier, η_{total}^{mat} .

According to Kotter, the total radiation efficiency could be given by expression 1 [25], where λ is the wavelength of the incident light and the upper and lower integration limits λ_{start} and λ_{stop} should cover the optical bandwidth for the solar energy harvesting.

$$\eta_{total}^{rad} = \frac{\int_{\lambda_{start}}^{\lambda_{stop}} P_{inc}(\lambda) \eta^{rad}(\lambda) d\lambda}{\int_{\lambda_{start}}^{\lambda_{stop}} P_{inc}(\lambda) d\lambda} \tag{1}$$

Furthermore, $P_{inc}(\lambda)$ is a function of the wavelength that follows Planck’s law for black body radiation according to expression 2, with T being the absolute temperature of the black body that in this case is the temperature of the surface of the sun, h the Planck’s constant, c the speed of light in vacuum, and k the Boltzmann constant.

$$P_{inc}(\lambda) = \frac{2\pi hc^2}{\lambda^5} \frac{1}{e^{\frac{hc}{\lambda kT}} - 1} \tag{2}$$

η^{rad} is the radiation efficiency of the antenna as a function of the wavelength that is given by expression 3, where P^{rad} , P^{inj} , and P^{loss} are the radiated power, the power injected at the terminals, and the power dissipated in the metal of the nanoantenna, respectively.

$$\eta^{rad} = \frac{P^{rad}}{P^{inj}} = \frac{P^{rad}}{P^{rad} + P^{loss}} \tag{3}$$

In order to generate DC power in the load, a rectifier is connected to the input port to rectify the current flowing in the antenna’s structure that oscillates around hundreds of THz. Like the total radiation efficiency, it is also possible to define the total matching efficiency as described on expression 4, where η^{mat} is the matching efficiency of the nanoantenna rectifier system given by expression 5, with Z_{rec} being the impedance of the rectifier and Z_{ant} the

input impedance of the nanoantenna. Moreover, R_{rec} is the real part of the impedance of the rectifier and R_{ant} the real part of the nanoantenna input impedance.

$$\eta_{total}^{mat} = \frac{\int_{\lambda_{start}}^{\lambda_{stop}} P_{inc}(\lambda) \eta^{rad}(\lambda) \eta^{mat}(\lambda) d\lambda}{\int_{\lambda_{start}}^{\lambda_{stop}} P_{inc}(\lambda) \eta^{rad}(\lambda) d\lambda} \tag{4}$$

$$\eta^{rad} = \frac{4R_{rec}R_{ant}}{|Z_{rec} + Z_{ant}|^2} \tag{5}$$

All these quantities are marked in Figure 6, an equivalent circuit of the total rectenna system, where both the transmitting and receiving processes can be easily described.

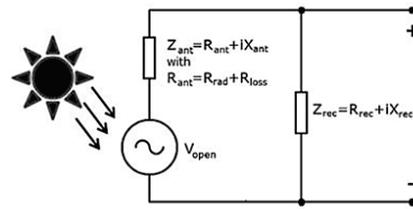


Figure 6. Equivalent circuit for the rectenna system (adapted from the work in [5]).

V_{open} is the voltage generated by the receiving antenna at its open terminals, while V_{rec} is the voltage seen at the terminals when a current is flowing to the rectifier. The useful power is the power going to the impedance of the rectifier Z_{rec} and it is given by expression 6.

$$P_{rec} = \frac{R_{rec}}{2} \frac{V_{open}^2}{|Z_{rec} + Z_{ant}|^2} \tag{6}$$

This power is maximal under optical matching conditions, i.e., $Z_{rec} = Z_{ant}^*$, leading to expression 7.

$$P_{rec} = \frac{V_{open}^2}{8R_{ant}} \tag{7}$$

Finally, to define the total rectenna efficiency, η_{total}^{rec} , presented on expression 8, is just needed to sum expressions 1 and 4.

$$\eta_{total}^{rec} = \eta_{total}^{rad} \eta_{total}^{mat} \tag{8}$$

6. Model: Solar Cell

A solar cell, shown in Figure 7, is a PIN structure device with no voltage directly applied across the junction. The solar cell converts light into electrical power and delivers this power to a load. This process requires a material that can absorb the light photons. The interaction of an electron with a photon leads to the promotion of an electron from the valence band into the conduction band leaving behind a hole, i.e., the absorption of a photon by a semiconductor material results in the generation of an electron–hole pair. After an electron–hole pair is created, the electron and the hole move from the solar cell into an external circuit, producing a photocurrent I . The electron then dissipates its energy in the external circuit and returns to the solar cell [26–42].

Some processes illustrated in Figure 7 are (1) absorption of a photon leads to the generation of an electron–hole pair; (2) recombination of electrons and holes; (3) electrons and holes can be separated with semipermeable membranes; (4) the separated electrons can be used to drive an electric circuit; and (5) after all electrons passed through the circuit, they will recombine with holes.

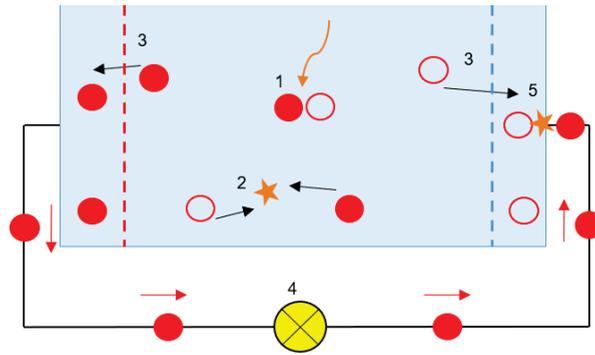


Figure 7. Simple model a solar cell connected to a load (sourced from the work in [43]).

That solar cell is a PIN junction, also illustrated in Figure 8. The PIN structure consists of a p region and a n region separated by an intrinsic layer. The p region and n region have different electrons concentration: the n-type has an excess of electrons while the p-type has an excess of holes, i.e., positive charges. The intrinsic layer width W is much larger than the space charge width of a normal PN junction [28–42].

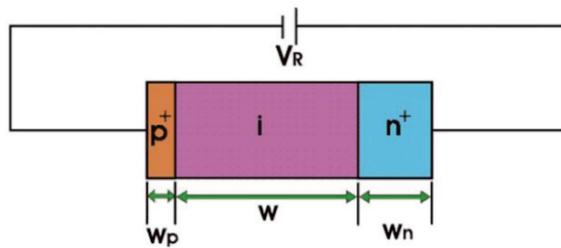


Figure 8. Circuit of a PIN junction, where W is the intrinsic width.

Absorption of light occurs in the intrinsic zone. A voltage V_R is applied so that there is an electric field in the intrinsic zone large enough so when the photons are absorbed, an electron–hole pair is created, i.e., a negative charge, electron, goes to the conduction band of the semiconductor and in the valence band a positive charge is going to move on the action of the electric field [28–42]. Therefore, there is an electric field that immediately separates the positive from the negative charge (the negative goes to one of the terminals and the positive one goes to the other).

The output of the PV cell is often represented with the relation between the current and voltage. This is known as the current–voltage curve (I–V curve). The I–V curve, represented in Figure 9, is a snapshot of all the potential combinations of current and voltage possible from a cell under standard test conditions (STC) [28–44]: (i) cell temperature: 25 °C (298.16 K); (ii) incident irradiance on the cell: $G = 1000 \text{ W m}^{-2}$; and (iii) spectral distribution of solar radiation: AM 1.5 spectrum.

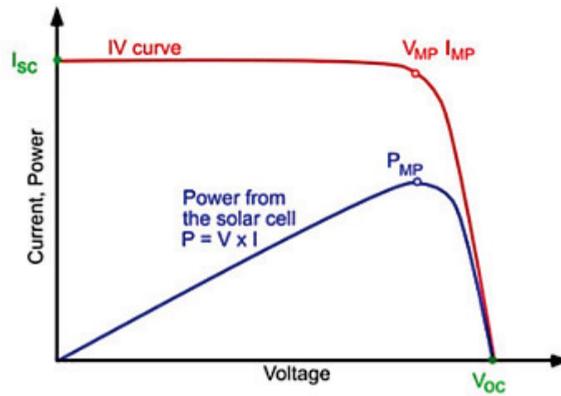


Figure 9. I–V curve (red) and power curve (blue) of a solar cell (sourced from the work in [45]).

The point in the I–V curve at which the maximum power is attainable is called Maximum Power Point (MPP), being that power calculated by expression 9 [28–42].

$$P_{MP} = V_{MP} \times I_{MP} \tag{9}$$

The representation of equipment through equivalent electrical circuits is a technique used in the field of electrical engineering. In order to study the PV equipment, a simplified electrical model is presented in Figure 10 [28–42].

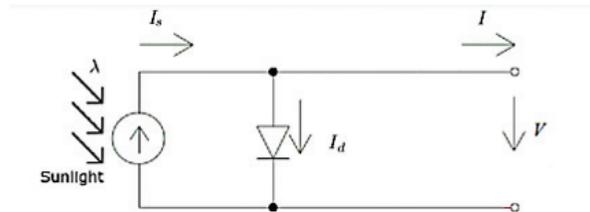


Figure 10. Equivalent circuit of a PV cell (1 diode and 3 parameters model-1M3P).

This model has three parameters: I_s , I_0 , and n .

I_s , also known as I_{pv} , represents the electric current generated by the beam of light radiation, consisting of photons, upon reaching the active surface of the cell. The level of this current depends on the irradiance [28–42].

The PIN junction functions as a diode that is traversed by an internal unidirectional current I_d which depends on the voltage V at the terminals of the cell and on the parameters I_0 and n , as it is possible to verify from expression 10 [28–42].

$$I_d = I_0 \left(e^{\frac{V}{n v_T}} - 1 \right) \tag{10}$$

Then, I_0 is the reverse saturation current of the diode, n is the diode ideality factor and v_T is the thermal voltage for a given temperature, determined using expression 11, from the Boltzmann’s constant, k , and electron charge value, q [28–42].

$$v_T = \frac{kT}{q} \tag{11}$$

Using the Kirchhoff's Current Law (KCL) on that internal node, expression 12 is revealed [28–42].

$$I = I_s - I_d = I_s - I_0 \left(e^{\frac{V}{nV_T}} - 1 \right) \quad (12)$$

However, the simplified model of 1 diode and 3 parameters is not a strict representation of the PV cell. It is necessary to take into account the voltage drop in the circuit up to the external contacts, which can be represented by a series resistance R_s and also the leakage currents, which can be represented by a parallel resistance, R_p . The influence of these parameters on the I–V characteristic of the solar cell can be studied using the equivalent circuit presented on Figure 11 [28–42].

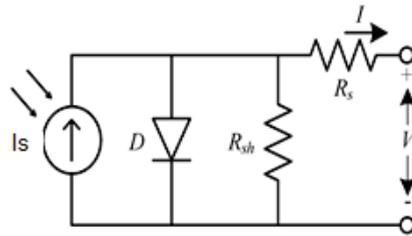


Figure 11. Equivalent circuit of a PV cell (1 diode and 5 parameters model-1M5P).

The model parameters are I_s , I_0 , n , R_s , and R_p , and thus the output current can be related to the output voltage based on expression 13 [28–42].

$$I = I_s - I_d - I_{R_p} = I_s - I_d = I_s - I_0 \left(e^{\frac{V}{nV_T}} - 1 \right) - \frac{V + R_s I}{R_p} \quad (13)$$

7. Simulation Results

In this section, a set of simulations are going to be presented. The main software used for this study was COMSOL Multiphysics®. It is generally used for modeling and simulation of real-world multiphysics systems.

First, we begin to module a PIN junction (solar cell). The purpose of the simulation is to study the propagation of light inside the semiconductor device. The incident light, an EM wave with a wavelength of 530 nm in the visible band, hits a silicon PIN junction with dimensions 150 nm, length of the p-junction; 2 μm, length of the intrinsic layer; and 80 nm, length of the n-junction. The width is 0.5 μm, while the PIN junction depth is 640 nm. These values are representative for a 0.35 μm CMOS process.

The geometry consists of two parts: the first part is air (in gray), whose edge on top is used as the source for the EM wave that arrives to the solar cell, and the second part, in blue, is the PIN junction (from top to bottom, n-junction, intrinsic zone, and the p-junction).

The results are obtained through the simulations performed on COMSOL Multiphysics®, which uses the finite element method (FEM). This is a numerical method for solving problems of engineering and mathematical physics. To solve a problem, it subdivides a large system into smaller, simpler parts called finite elements.

In this case, FEM is used to calculate the electric field, so that the program needs to define a mesh to solve the system of equations.

A customized mesh with triangular elements and a maximum element size of 10 nm was defined, as presented on Figure 12. The basic condition is that the mesh size should be lower than wavelength, in order not to have numerical errors in the calculation of the solution.

The parameters used for the mesh on the different simulations are represented on Table 1.

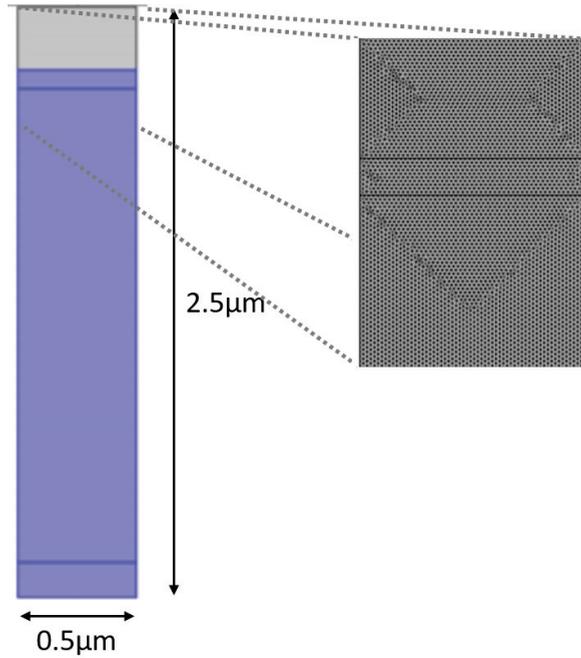


Figure 12. Schematic representation of a PIN junction on COMSOL Multiphysics®, as well as its mesh.

Table 1. Mesh parameters COMSOL Multiphysics®.

Parameter	Value
Maximum element size	1×10^{-8} [m]
Minimum element size	5×10^{-11} [m]
Maximum element growth rate	1.1
Curvature factor	0.2
Resolution of narrow regions	1

The mesh settings determine the resolution of the finite element mesh used to discretize the model. A higher value results in a finer mesh in narrow regions. In this example, because the geometry contains small edges and faces, an extremely fine mesh was designed. This will better resolve the variations of the stress field and give a more accurate result. Refining the mesh size to improve computational accuracy always involves some sacrifice in speed and typically requires increased memory usage [46].

This study is focus on the Transverse Electric (TE) polarization. TE polarized light is characterized by its electric field being perpendicular to the plane of incidence. For TE light, the magnetic field lies in the plane of incidence, thus its always perpendicular to the electric field in isotropic materials. On the other hand, Transverse Magnetic (TM) polarized light is characterized by its magnetic field being perpendicular to the plane of incidence [47].

In this case, the electric field has only one component along the z-direction (horizontal axis).

The PIN junction was tested for different values of λ (light wavelength): 400 nm (blue), 530 nm (green), and 800 nm (IR), as observed on Figure 13.

For a light wavelength of 400 nm, in the blue region, the photons are absorbed mainly in the top of the intrinsic region. The electric field is zero in the bottom part of the intrinsic region.

For a light wavelength of 530 nm, the electric field is stronger in the n-junction and decreases along the intrinsic zone, due to the fact that the photons are absorbed mainly in this area.

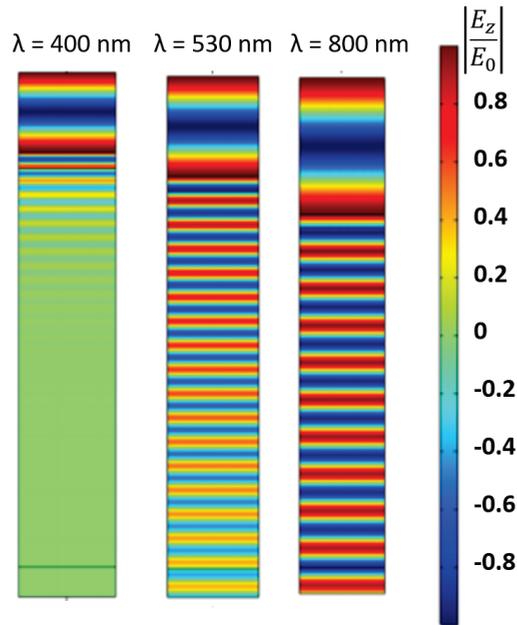


Figure 13. Normalized Electric field, z-component of the cross section of a PIN junction.

For a light wavelength of 800 nm, it is observed that the electric field practically does not decrease along the intrinsic zone. Thus, it is concluded that there is almost no absorption of photons for this wavelength.

When a nanoantenna with an array of air slits or apertures is introduced on top of the silicon PIN junction, the behavior of the electric field changes.

The main purpose of the simulations with a nanoantenna is to observe the difference between a PIN junction without nanoantenna and with a nanoantenna. Furthermore, it is our interest to analyze the evolution of the diffraction pattern as the number of air slits increases, namely, a three-slit, a seven-slit, and a fifteen-slit array, and to compare the simulation results with the results expected by the classical theory [48].

The simulation environment used is similar to that of Figure 12, where an incident light wave hits the PIN junction by propagating through the air slit arrays and absorbed along the intrinsic region.

Various experiments were performed, where the electric field was normalized to $E(0)$, that is, the incident electric field. The incident light wave has an electric field whose amplitude is registered. This amplitude is constant for all the simulated cases and thus it will serve for normalization. It is necessary to have a normalization constant in order to better compare the electric field values for the cases when there is a nanoantenna on top of the PIN junction and when there is no nanoantenna (the structure will be different).

When light hits the surface, the electric field is no longer the incident field. It is the incident field plus the reflected field, and the reflected field varies whether or not there is a nanoantenna.

In these experiments, it was considered that the dimensions of the air slits and their spacing had subwavelength dimensions as well as the metal thickness. Furthermore,

for four different values of the light wavelength, four particular cases were considered: (i) nanoantenna metal thickness, $\lambda/10$ and air slit width, $\lambda/10$; (ii) nanoantenna metal thickness, $\lambda/100$ and air slit width, $\lambda/2$; (iii) nanoantenna metal thickness, $\lambda/100$ and air slit width, $\lambda/5$; and (iv) nanoantenna metal thickness, $\lambda/100$ and air slit width, $\lambda/10$.

For each case, on top of the PIN junction a three-slit, a seven-slit, and a fifteen-slit array were tested. The procedures required to study and simulate a fifteen-slit array are identical to those used to simulate a three-slit or a seven-slit array. The parameters are the same, differing only in the number of slits. The maximum absolute values of the normalized electric field along the intrinsic region for an aluminum nanoantenna were registered on Table 2.

Table 2. Maximum absolute values of the normalized electric field along the intrinsic region.

Light Wavelength [nm]	Metal Thickness	Air Slit Width	3 Slits	7 Slits	15 Slits
400	$\lambda/10$	$\lambda/10$	0.087	0.069	0.860
400	$\lambda/100$	$\lambda/5$	0.536	0.369	0.577
400	$\lambda/100$	$\lambda/10$	0.335	0.356	0.517
530	$\lambda/10$	$\lambda/10$	0.190	0.181	0.122
530	$\lambda/100$	$\lambda/5$	1.019	1.018	1.040
530	$\lambda/100$	$\lambda/10$	0.956	0.893	0.908
800	$\lambda/10$	$\lambda/10$	0.188	0.098	0.140
800	$\lambda/10$	$\lambda/2$	1.787	2.575	2.633
800	$\lambda/100$	$\lambda/5$	1.704	2.547	1.612
800	$\lambda/100$	$\lambda/10$	1.605	1.010	1.027
1550	$\lambda/10$	$\lambda/10$	0.177	0.063	0.272
1550	$\lambda/10$	$\lambda/2$	10.053	8.071	5.806
1550	$\lambda/100$	$\lambda/5$	11.467	4.508	4.724
1550	$\lambda/100$	$\lambda/10$	2.304	1.369	1.083

When the total electric field is normalized by the incident field, it is possible to immediately check whether the radiation through the intrinsic region is higher or lower than the incident radiation. In other words, if any numerical value obtained by the different simulations is greater than 1, it means that the structure itself has the capacity to transmit more light than its incidence, which indicates the occurrence of the Extraordinary Optical Transmission phenomenon. The results highlighted in green indicate the occurrence of the EOT phenomenon.

The metal thickness $\lambda/100$ proved to be more efficient and thus more simulations were performed with this size. This metal thickness was the most efficient as it can be in part attributed to the fact that aluminum, for very small film thicknesses, has a very large transmission coefficient and a low reflection coefficient. Meanwhile, for a metal thickness of $\lambda/10$ there was no occurrence of the EOT phenomenon. Contrary to what happens in the previous case, in this case practically everything is reflected and little transmitted.

The results obtained from the simulations indicate that (i) if the nanoantenna metal thickness is much smaller in relation to the wavelength, the stronger will be the electric field intensity in the intrinsic region, and (ii) the smaller the air slit width in relation to the wavelength, the smaller the intensity of the electric field in the intrinsic region, as expected given the classical theories of diffraction.

These results are confirmed by the classical theory as EOT is observed mainly due to the constructive interference of SPPs propagating between the slits of the nanoantenna, where they can be coupled from/into radiation.

The shape, dimensions, and the spacing between apertures are fundamental parameters that must be carefully sized to allow the propagation of SPPs and the occurrence of the EOT phenomenon. With the aid of MATLAB software, a 1D plot was made to compare the

values of the normalized electric field along the intrinsic zone for the light wavelength of 400 nm with an aluminum nanoantenna and without nanoantennas.

It is observed in all cases that the electric field is stronger in the n-junction and then rapidly reaches the zero value in the middle of the intrinsic zone.

By analyzing Figure 14, it is observable that the normalized electric field is stronger without nanoantennas. For this light wavelength, the results for other parameters of metal thickness and air slit width in Table 2 are quite identical, and thus for a light wavelength of 400 nm, the introduction of nanoantennas for solar harvesting does not contribute for a bigger efficiency of the solar cell.

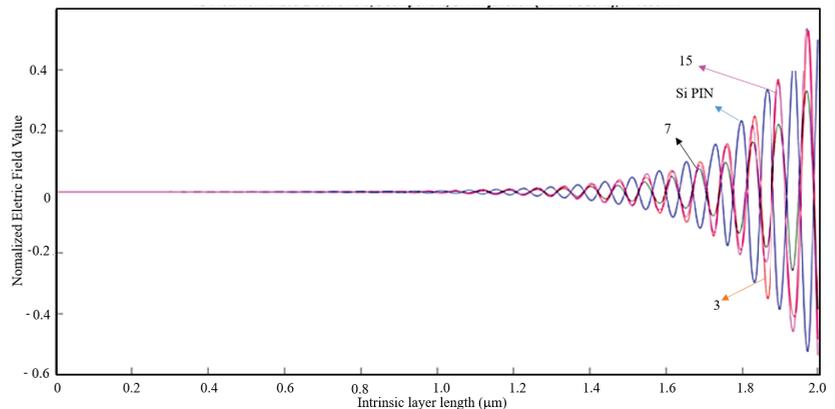


Figure 14. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for a light wavelength of 400 nm: Si PIN junction (blue); 3-slit array Al nanoantenna (red); 7-slit array Al nanoantenna (black); and 15-slit array Al nanoantenna (magenta).

Given a light wavelength of 530 nm, according to Table 2 for a metal thickness of $\lambda/100$ and an air slit width of $\lambda/5$ the EOT phenomenon barely occurs. Like in the previous case, a 1D plot was made on MATLAB and it is presented on Figure 15.

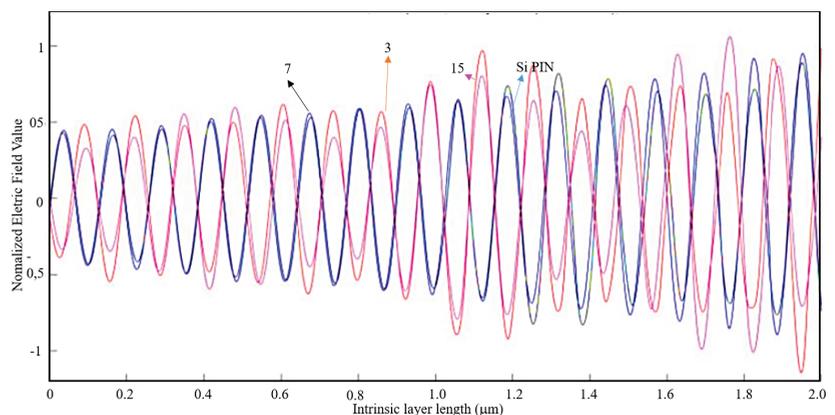


Figure 15. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for a light wavelength of 530 nm: Si PIN junction (blue); 3-slit array Al nanoantenna (red); 7-slit array Al nanoantenna (black); and 15-slit array Al nanoantenna (magenta).

It is observable on Figure 15 that the results obtained for the normalized electric field with and without an aluminum nanoantenna are very similar. Therefore, one can conclude

that for 530 nm of light wavelength the introduction of nanoantennas for solar harvesting barely contributes for a bigger efficiency of the solar cell.

For a light wavelength of 800 nm, the EOT phenomenon does not occur if the metal thickness is $\lambda/10$. For a metal thickness of $\lambda/100$, the EOT phenomenon occurs for every case and thus it is concluded that the nanoantennas are indeed efficient for this wavelength where $\lambda/100$ is the optimum thickness (see Table 2).

Below in Figures 16–18, the cases where the EOT phenomenon occurs are represented.

By analyzing Figure 16, although the 15-slit array nanoantenna has recorded the maximum absolute value of the normalized electric field, the seven-slit array is the most efficient nanoantenna type, as the normalized electric field is higher along the entire intrinsic zone.

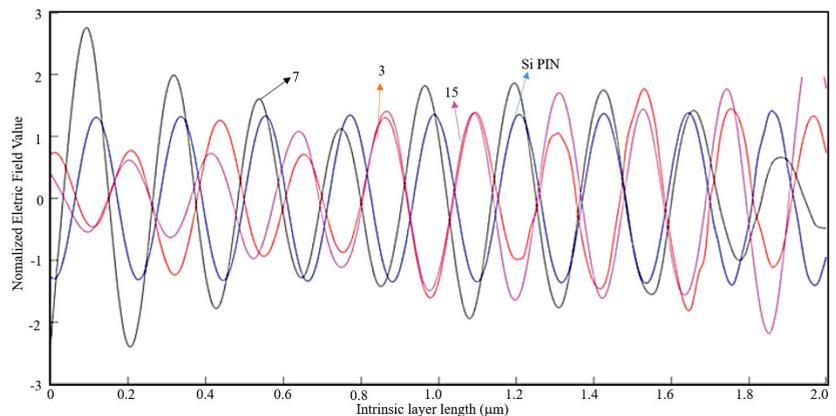


Figure 16. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for a light wavelength of 800 nm (metal thickness: $\lambda/100$; air slit width: $\lambda/2$).

By analyzing Figure 17, one can conclude that a seven-slit array is the most efficient along the intrinsic zone, and from Figure 18, it is concluded that it is the three-slit array.

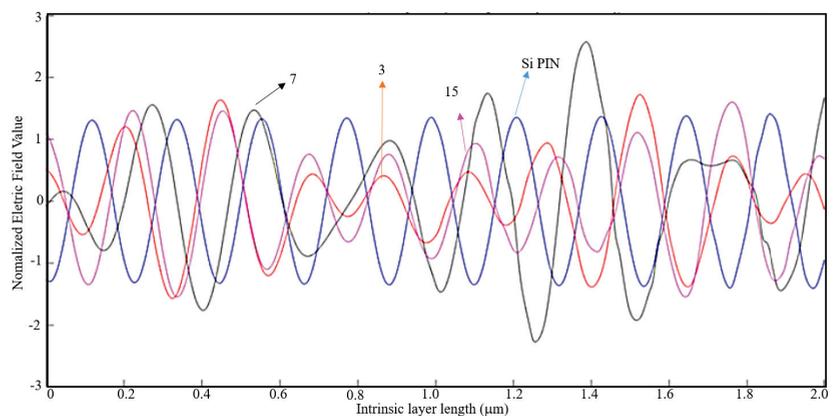


Figure 17. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for a light wavelength of 800 nm (metal thickness: $\lambda/100$; air slit width: $\lambda/5$).

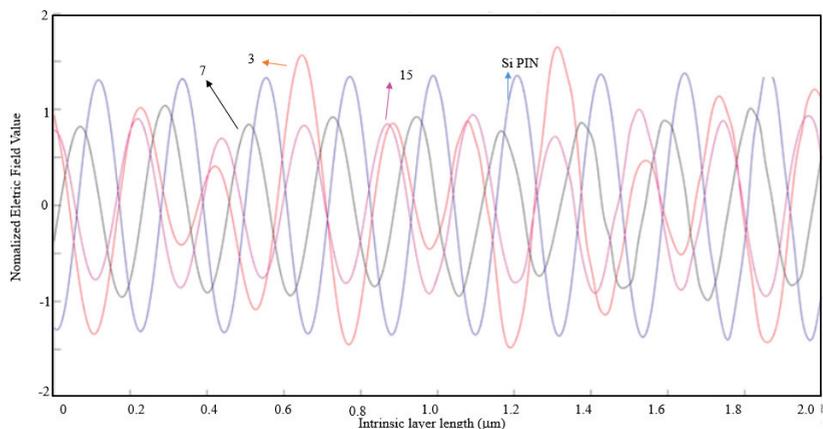


Figure 18. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for a light wavelength of 800 nm (metal thickness: $\lambda/100$; air slit width: $\lambda/10$).

Even though there is the occurrence of EOT, the nanoantennas are less efficient for this air slit width and thus there is no visible advantage on their implementation.

The procedures that are necessary to carry out the study and simulation of an array of slits with different material types are identical to those used previously. The metals that will be considered in the following simulations using the COMSOL Multiphysics® software are Gold (Au) and Platinum (Pt).

In Tables 3 and 4 are registered the maximum absolute values of the normalized electric field along the intrinsic region for a nanoantenna of gold and for another of platinum, respectively, on top of a silicon PIN junction.

Table 3. Maximum absolute values of the normalized electric field along the intrinsic region for a gold nanoantenna.

Light Wavelength [nm]	Metal Thickness	Air Slit Width	3 Slits	7 Slits	15 Slits
400	$\lambda/10$	$\lambda/10$	0.228	0.340	0.171
400	$\lambda/100$	$\lambda/5$	0.539	0.541	0.483
400	$\lambda/100$	$\lambda/10$	0.571	0.570	0.522
530	$\lambda/10$	$\lambda/10$	0.657	0.913	0.302
530	$\lambda/100$	$\lambda/5$	1.078	0.955	0.902
530	$\lambda/100$	$\lambda/10$	0.932	0.928	0.900
800	$\lambda/10$	$\lambda/10$	0.755	0.235	0.318
800	$\lambda/100$	$\lambda/5$	1.392	1.413	1.612
800	$\lambda/100$	$\lambda/10$	1.083	1.058	1.280
1550	$\lambda/10$	$\lambda/10$	0.045	0.076	0.207
1550	$\lambda/100$	$\lambda/5$	3.441	4.489	2.810
1550	$\lambda/100$	$\lambda/10$	1.503	1.407	2.525

Table 4. Maximum absolute values of the normalized electric field along the intrinsic region for a platinum nanoantenna.

Light Wavelength [nm]	Metal Thickness	Air Slit Width	3 Slits	7 Slits	15 Slits
400	$\lambda/10$	$\lambda/10$	0.130	0.223	0.152
400	$\lambda/100$	$\lambda/5$	0.584	0.578	0.569
400	$\lambda/100$	$\lambda/10$	0.572	0.578	0.969
530	$\lambda/10$	$\lambda/10$	0.210	0.411	0.197
530	$\lambda/100$	$\lambda/5$	1.013	1.002	0.994
530	$\lambda/100$	$\lambda/10$	1.215	0.957	0.968
800	$\lambda/10$	$\lambda/10$	0.191	0.139	0.145
800	$\lambda/100$	$\lambda/5$	1.588	1.591	1.243
800	$\lambda/100$	$\lambda/10$	1.261	1.048	1.105
1550	$\lambda/10$	$\lambda/10$	0.053	0.011	0.031
1550	$\lambda/100$	$\lambda/5$	1.633	1.726	2.333
1550	$\lambda/100$	$\lambda/10$	1.317	1.253	1.234

From the observation of both tables above, and comparing the results with an aluminum nanoantenna in Table 2, one can verify that the EOT phenomenon is present in all material types. In addition, it is possible to observe that the EOT phenomenon is stronger with an aluminum nanoantenna, as maximum absolute values of the normalized electric field along the intrinsic region of $10 \times$ the incident field were registered for a three-slit array.

For a gold or a platinum nanoantenna, the results obtained show that the EOT phenomenon is mostly present for the light wavelengths of 800 nm and 1550 nm. These results show clear evidence of the EOT phenomenon and constitute an interesting result for the implementation of an aperture nanoantenna, as the electric field in the near-field region is strongly enhanced.

In Figure 19, the case where the maximum absolute value of the normalized electric field along the intrinsic region for an aluminum nanoantenna on top of a Si PIN junction had the highest value, as compared with the other nanoantenna material types. From the observation of Figure 19, it is clearly visible the difference of the normalized electric field along the intrinsic zone for the aluminum nanoantenna and the other material types.

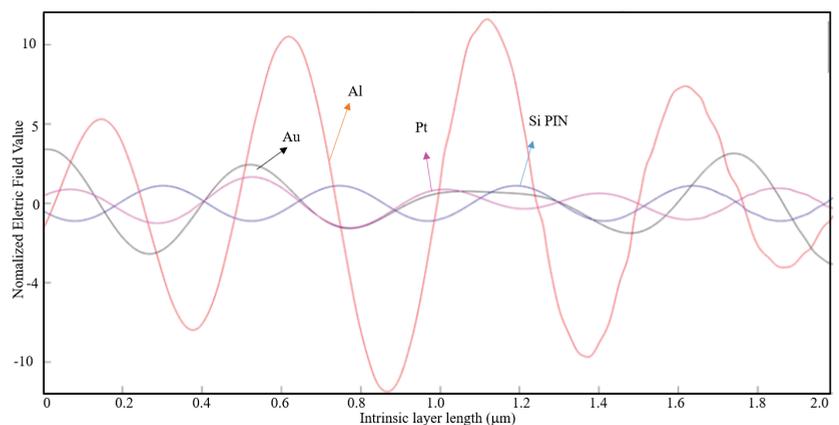


Figure 19. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for different nanoantenna material types: Si PIN junction (blue), Al nanoantenna (red), Au nanoantenna (black), and Pt nanoantenna (magenta) (3-slit array; light wavelength: 1550 nm; metal thickness: $\lambda/100$; and air slit width: $\lambda/5$).

For the same parameters, in Figures 20 and 21 are represented the simulation results for a seven-slit array and a fifteen-slit array nanoantenna, respectively, for the three materials types and the Si PIN junction.

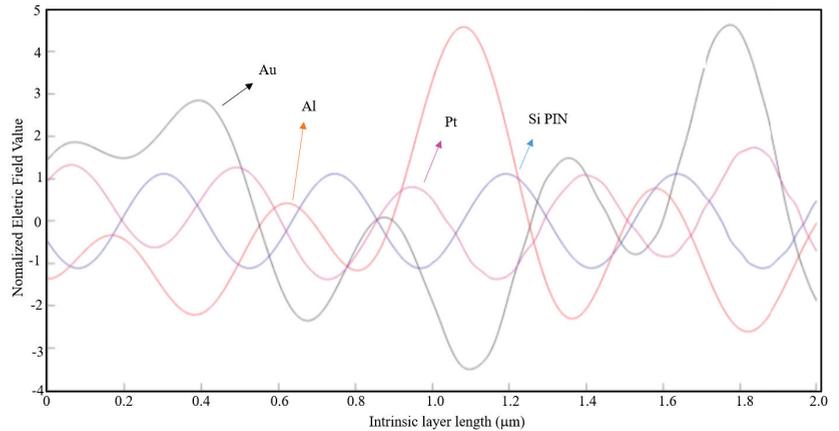


Figure 20. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for different nanoantenna material types: Si PIN junction (blue), Al nanoantenna (red), Au nanoantenna (black), and Pt nanoantenna (magenta) (7-slit array; light wavelength: 1550 nm; metal thickness: $\lambda/100$; air slit width: $\lambda/5$).

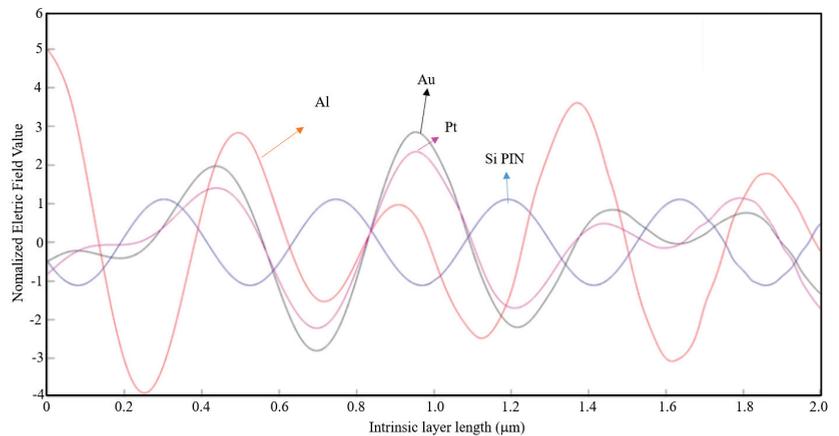


Figure 21. 1D Plot of the normalized electric field, z-component, along the intrinsic zone for different nanoantenna material types: Si PIN junction (blue), Al nanoantenna (red), Au nanoantenna (black), and Pt nanoantenna (magenta) (15-slit array; light wavelength: 1550 nm; metal thickness: $\lambda/100$; air slit width: $\lambda/5$).

By analyzing these figures, it is verified that the aluminum and the gold nanoantenna have by far a stronger normalized electric field along the entire intrinsic region compared to the platinum nanoantenna and the case without any nanoantennas. Comparing the three cases above, one can conclude that aluminum is the most appropriate material for the application of an optical antenna.

8. Study of the Short-Circuit Current and the Open-Circuit Voltage on the Solar Cell

As previously referred, a solar cell can be modeled using the single diode and 3 parameters model, that includes the I–V and the P–V characteristics of a typical module.

The problem of modeling a PV system is further compounded by the fact that the I–V curve of a PV module is dependent on the irradiance and temperature, which are continuously changing. Consequently, the parameters required to model a PV module must be adjusted according to the ambient temperature and irradiance [43]. Two main parameters that are used to characterize the performance of a solar cell are the short-circuit current, I_{sc} , and the open-circuit voltage, V_{oc} .

In order to prove that the model used during the simulations on COMSOL Multiphysics® is indeed a solar cell, the short-circuit current and the open-circuit voltage were measured upon variation of the irradiance and temperature. As the software does not simulate directly the short-circuit current in the cell, a simulation of the current density norm, J_{sc} , was made. In this simulation, the solar cell was short-circuited as depicted in Figure 22.

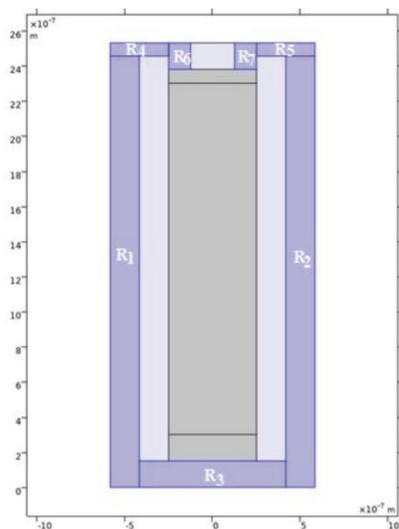


Figure 22. Short-circuited solar cell model (gray: Si PIN junction; dark blue: aluminum; light blue: Air).

According to Ibrahim, the complete equation for the short-circuit current, taking into account that it varies with the irradiance and the temperature on the solar cell, is described by expression 14, where α_{STC} is the thermal coefficient of the short-circuit current, measuring the variation of I_{sc} with an increase of 1 °C of temperature T [49].

$$I_{sc}(G, T) = \frac{G}{G_{STC}} [I_{sc_{STC}} + \alpha_{sc}(T - T_{STC})] \tag{14}$$

Although COMSOL can simulate the variation in the temperature, during the simulations the temperature T on the PV cell is considered to be constant and equal to STC. Considering that the software does not simulate directly the short-circuit current in the cell, but the current density norm, given by expression 15.

$$J_{sc} = \frac{G}{G_{STC}} J_{sc_{STC}} \tag{15}$$

Table 5 contains the average values of the current density norm with the input irradiance.

Table 5. Values of the current density norm with the input irradiance.

Irradiance [W m^{-2}]	$J_{sc_{min}}$ [$\times 10^6 \text{ A m}^{-1}$]	$J_{sc_{max}}$ [$\times 10^6 \text{ A m}^{-1}$]	$J_{sc_{avg}}$ [$\times 10^6 \text{ A m}^{-1}$]
400	0.88	10.05	5.47
500	0.92	11.25	6.09
600	1.00	12.33	6.67
700	1.10	13.30	7.20
800	1.20	14.20	7.70
900	1.25	15.10	8.18
1000	1.29	15.97	8.63
1100	1.35	16.78	9.07
1200	1.40	17.60	9.50
1300	1.48	18.33	9.91
1400	1.60	18.96	10.28

From Figure 23, the current density norm varies almost linearly with the input irradiance for this range of values on the PV cell. The slight nonlinearity can be attributed to the resistance of the material (in this case, aluminum). The resistance of any material is a function of the material's resistivity, ρ , and the material's dimensions, and it is given by expression 16, where L , t , and W are the length, the thickness, and the width of the material, respectively [43].

$$R = \frac{\rho L}{tW} \quad (16)$$

As presented on Figure 22, there are 7 blocks or sections of aluminum surrounding the solar cell (in order to perform a short-circuit of the PV cell). Based on expression 16, it is possible to determine the value of that blocks resistance, which is presented on Table 6, for a $\rho(T = 25^\circ\text{C}) = 2.70 \times 10^{-8} \Omega \text{ m}$ and $t = 640 \text{ nm}$.

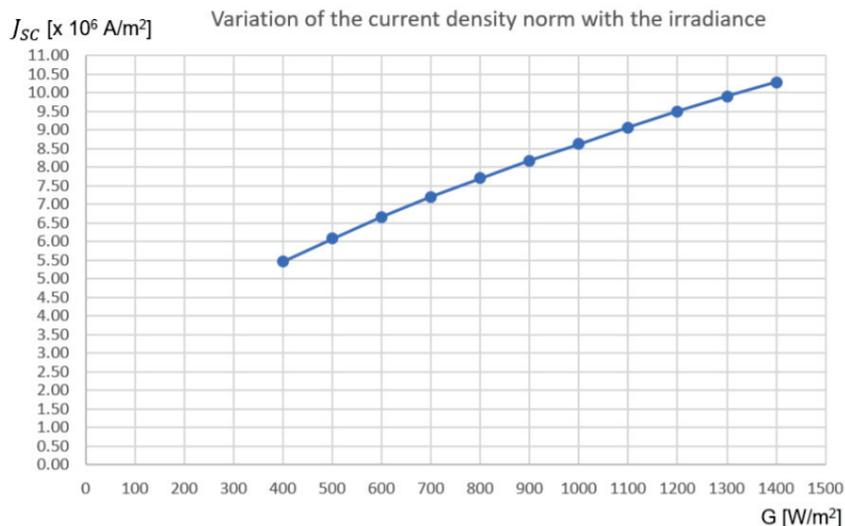


Figure 23. 1D Plot of the variation of J_{sc} with the irradiance (x-axis: Irradiance [W/m^2]; y-axis: Average value of the current density norm, $J_{sc_{avg}}$ [$\times 10^6 \text{ A m}^{-1}$]).

Table 6. Aluminum sections dimensions and resistance value.

Section	Length, L [m]	Width, W [m]	Resistance, R [mΩ]
R ₁	2.455×10^{-6}	1.666×10^{-7}	621.447
R ₂	2.455×10^{-6}	1.666×10^{-7}	621.447
R ₃	150×10^{-9}	8.335×10^{-7}	7.692
R ₄	0.075×10^{-6}	3.336×10^{-7}	9.485
R ₅	0.075×10^{-6}	3.336×10^{-7}	9.485
R ₆	150×10^{-9}	1.250×10^{-7}	50.625
R ₆	150×10^{-9}	1.250×10^{-7}	50.625

By analyzing the values of the resistance for each block of aluminum, one can conclude that the resistance is an important factor to consider. All the values obtained for the resistance of each block are in agreement with the 0.35 μm CMOS process. Therefore, the nonlinearity of the current density norm with the input irradiance is explained.

Similar to the procedure to the I_{sc} , it is possible to verify how V_{oc} varies with the irradiance, as verified on Table 7.

Table 7. Values of the open-circuit voltage with the input irradiance.

Irradiance [W m ⁻²]	V_{bot} [V]	V_{bot} [V]	V_{oc} [V]
100	−4.5189	−5.3311	0.8121
200	−4.5189	−5.3311	0.8121
400	−4.5189	−5.3311	0.8121
800	−4.5189	−5.3311	0.8121
1000	−4.5189	−5.3311	0.8121
1200	−4.5189	−5.3311	0.8121

The open-circuit voltage has a steady value equal to 0.8121 V, for different values of the irradiance, G, leading to the conclusion that it is not dependent on the irradiance. This value is the maximum voltage the solar cell on this model can deliver.

The open-circuit voltage varies with the irradiance by expression 17, leading to the conclusion that this variations is not very significant, because it follows a logarithmic function, where N_s is the number of series-connected cells in a PV module (if it is a single PV cell, this value is equal to 1) and α_{oc} is the thermal coefficient of the open-circuit voltage.

$$V_{oc}(G, T) = V_{oc_{STC}} + \frac{N_s k T}{q} \ln(G) + \alpha_{oc}(T - T_{STC}) \quad (17)$$

To conclude, the short-circuit current, I_{sc} , varies nonlinearly with irradiance and its variation with temperature is fairly small depending on its temperature coefficient. When determining the dependence of the open-circuit voltage, V_{oc} , on temperature and irradiance, it is found that it is strongly dependent only on the temperature. It has been observed that the results obtained in this study are in accordance with what is expected by the classical theory of a photovoltaic cell and so the model that was tested on COMSOL software is valid.

9. Conclusions

The main objective of this article is the study and simulation of the behavior of an optical antenna with subwavelength dimensions for solar harvesting on PV panels. To perform such study, the COMSOL Multiphysics® software was used, to obtain the simulation numerical results of the studied structures.

It has been demonstrated with several simulations in different conditions that the EOT phenomenon was always confirmed on nanoantennas with three materials: aluminum (Al), gold (Au), and platinum (Pt). Thus, it means that these structures have the capacity to transmit more light than its incidence, in orders of magnitude greater than predicted by standard

aperture theory. These experiments provide evidence that these unusual optical properties are due to the coupling of light with SPPs on the surface of the metallic nanoantennas.

Additionally, it has been verified with the simulation results that optimum results were obtained for light wavelengths of 800 nm and 1550 nm. These results constitute an interesting result for the implementation of an aperture nanoantenna, as they cover a wide range of the spectrum: the EOT phenomenon was verified on almost the entire visible region as well as the IR region. Typical silicon solar cells have proven to be inefficient at these wavelengths.

Although most of the researchers use gold or silver to fabricate the optical antennas, the results obtained in this article show that aluminum can have even better results than the other material types, mainly due to its transmission and reflection coefficients. Furthermore, among all metals analyzed, aluminum has the smallest skin depth in the visible spectrum, as well as being cheaper than gold or platinum. However, aluminum is unstable. It oxidizes quickly, and the optical properties are lost. Therefore, aluminum has to be coated with an antioxidant compound.

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Review

A Brief Review of the Role of 2D Mxene Nanosheets toward Solar Cells Efficiency Improvement

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Abstract: This article discusses the application of two-dimensional metal MXenes in solar cells (SCs), which has attracted a lot of interest due to their outstanding transparency, metallic electrical conductivity, and mechanical characteristics. In addition, some application examples of MXenes as an electrode, additive, and electron/hole transport layer in perovskite solar cells are described individually, with essential research issues highlighted. Firstly, it is imperative to comprehend the conversion efficiency of solar cells and the difficulties of effectively incorporating metal MXenes into the building blocks of solar cells to improve stability and operational performance. Based on the analysis of new articles, several ideas have been generated to advance the exploration of the potential of MXene in SCs. In addition, research into other relevant MXene suitable in perovskite solar cells (PSCs) is required to enhance the relevant work. Therefore, we identify new perspectives to achieve solar cell power conversion efficiency with an excellent quality–cost ratio.

Keywords: power conversion efficiency; solar cells; MXenes; electrodes; additives; HTL/ETL

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1. Introduction

The development of innovative materials for efficient solar cells has garnered a lot of attention [1–10] because of the ever-increasing need for renewable and clean energy supplies [11–15]. Sunlight has been identified as the most prevalent, cheapest, and cleanest source of energy for meeting society's long-term energy requirements. Solar cells convert sunlight directly into electricity—the most efficient and practical method to utilise solar energy. Earth-rich silicon (Si)-based solar cells dominate the industry, with power conversion efficiencies (PCEs) of over 26 percent and a 25-year average module living standard [16–18]. However, since Si solar cells have high initial production costs, researchers are turning their attention to less expensive alternatives, such as perovskite solar cells (PSCs), organic solar cells (OSCs), quantum dot solar cells (QDSCs), and dye-sensitised solar cells (DSSCs) [19].

PSCs are the most feasible option among these new PV technologies for providing a PCE equivalent to maturing silicon solar cells. Furthermore, compared to traditional Si-based technologies, their lower costs, adjustable band gap, processability at low temperatures, long charge carrier diffusion lengths, high light absorption coefficients, lower exciton binding energy, numerous options for much simpler mass production processes lacking additional advantages, and increasing performance make it a more lucrative option [20–26]. Additionally, in contrast to traditional Si solar cells, PSCs operate well even in diffuse or weak light, making them suitable for specialised purposes [27]. Due to the development of various architectures, chemical compositions, manufacturing protocols, advances in

materials, and phase stabilisation techniques, efficiencies have increased dramatically since the first report on all-solid-state PSCs in 2012, from 9.7% in 2012 to 25.5% percent in 2021 [28–31]. Between the highest observed efficiency and its theoretical maximum, PSCs may be split into two categories: the normal (n-i-p) structure and the inverted (p-i-n) structure [32,33].

Furthermore, concerns regarding PSC stability have been highlighted because a thin-film solar device must pass the IEC 61,646 environment stability test before it can be sold commercially [34]. A lot of research is now underway to improve the stability and performance of PSCs [19]. Scientists have been attempting to integrate perovskite into solar cells since the material's initial breakthrough in 2009. The solar cells in this material are more efficient than those in current solar modules [35]. On average, existing solar modules capture 15 to 18 percent of the sun's energy, while perovskite solar cells have an efficiency of up to 28 percent [36]. Dou's research team developed a sandwich-like material that mixes organic and inorganic components to form a composite structure that does not need lead and improves stability considerably. According to Yao Gao, the new organic-inorganic hybrid perovskite materials are cheaper and perform better than traditional inorganic semiconductors. Solar cells can be highly efficient using this new method; the authors made hybrid perovskite materials that are intrinsically more stable. These novel materials are better for the environment and safer for bioelectronic sensors on humans because the researchers removed hazardous lead [37].

Transition-metal nitrides, or carbides (MXenes), were first found in 2011 by Gogotsi and his coworkers as star materials from MAX phases, which are layered compounds resembling graphite with monoatomic A element layers sandwiched between electrically conductive and stiff MX-blocks [38–40]. It was proposed that the generated material be labelled MXenes to highlight the removal of the A element from the MAX phase and its two-dimensional (2D) shape, related to graphene. The material has recently shown promising applications in solar cells [41–44], biomedical fields [45–47], light-emitting diodes [48–50], sensors [51–55], energy storage [56–62], catalysis [63–66], water purification [67–72], and electromagnetic applications [41–44,73]. The nanoengineering of these 2D materials is a hot topic right now. Due to its adjustable work function, high electrical conductivity, good transparency, and charge-carrier mobility, $Ti_3C_2T_x$ (T stands for certain surface-terminating functional groups such as O, OH, and F) leads the current research on MXene in solar cells [74–76]. MXenes are currently divided into transition metals in either an out-plane or in-plane ordered form. Furthermore, most 2D transition-metal MXenes exist in the form of random solid solutions, which are characterised by two randomly distributed transition metals across the 2D structure. This review paper detailed the basic principles for the creation of each 2D transition-metal MXene structure, as well as their tunable characteristics depending on the transition-metal composition. 2D transition-metal MXenes vary from their counterparts mono-transition-metal MXenes, where two transition metals can occupy the metal sites.

Guo and his group included $Ti_3C_2T_x$ as an additive in the photoactive layer of methylammonium lead iodide (MAPbI₃) in the first research on MXene materials in perovskite solar cells, which was published in 2018 [77]. Since then, its application has been extended to the electrode, electron transport layer (ETL)/hole transport layer (HTL). The $Ti_3C_2T_x$ functions on MXenes in solar cell applications may be classified into three categories: electrode [78], additive [77], and ETL/HTL [79,80]. Figure 1 below summarises the synthesis, properties, and application of MXene. The solar cells (SCs) in Figure 1 have been widely investigated [73].

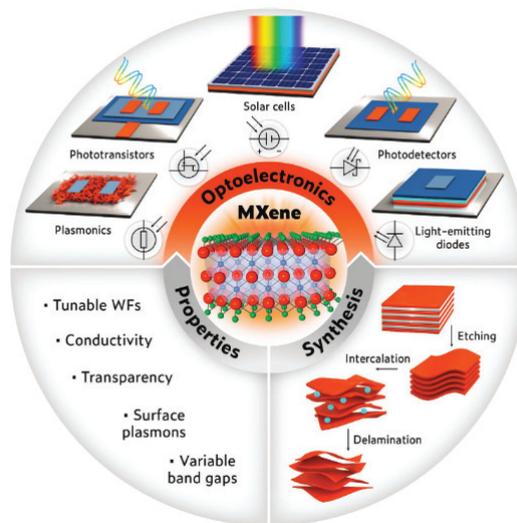


Figure 1. MXene synthesis, properties, and their applications. Reprinted with permission from ref. [73]. Copyright 2021 John Wiley & Sons, Inc.

This article summarises all previously reported work on incorporating MXene into solar cells to improve solar power generation and operational stability. The next section defines the efficiency improvement of SC and how it is classified. Section 3 lists the types of roles that MXene mainly plays in solar cells. A conclusion and prospect are given in Section 4.

2. The Efficiency Improvement of Solar Cells

The conversion efficiency of a solar cell is a measurement of incident light that can be converted to electrical energy. The incident light's power is the denominator, while the solar cell's electrical power is the numerator; thus, this conversion efficiency may be expressed as a fraction [77].

The power conversion efficiency (PCE) of solar cells is one of the most significant parameters [81]. The PCE has improved rapidly since the PSC's introduction in 2009 [82]. The PCE of Kojima et al. initial's PSC was just 3.8 percent [83]. Im et al. [84] claimed a PCE of 6.5 percent in 2011, while Kim et al. [28] recorded a PCE of nearly 9 percent in 2012. In 2016, approximately 22% of PCEs were verified, to the best of our knowledge [85]. All of these remarkable outcomes and conclusions in such a short period of time demonstrated PSC's tremendous potential [86]. Below is the equation used to calculate the conversion efficiency:

$$\text{Conversion efficiency (\%)} = \frac{\text{Generated electrical power (W)}}{\text{Incident light power (W)}} \times 100 \quad (1)$$

Fu et al. published a paper in 2019 that can be applied to various MXene compositions as possible electrodes for the creation of high-performance solar cells. Solar cells with a maximum power conversion efficiency (PCE) of 11.5 percent were delaminated from a few stacked $\text{Ti}_3\text{C}_2\text{T}_x$ MXene-contacted Si layers [87]. The authors recently suggested integrating an inorganic 2D Cl-terminated Ti_3C_2 ($\text{Ti}_3\text{C}_2\text{Cl}_x$) MXene into the volume and surface area of CsPbBr_3 Im to substantially decrease the superficial lattice tension. The faulty surface is healed, and a champion efficiency of 11.08 percent is obtained with an ultra-high open-circuit voltage of up to 1.702 V on the fully inorganic CsPbBr_3 -PSC, which is the greatest efficiency record for this kind of PSC to date. In addition, at 80 percent

relative humidity for 100 days and 85 degrees Celsius for 1 month, the unencapsulated device performs nearly as well as the enclosed device [86]. Y. Zhang et al. used density functional theory calculations to thoroughly assess 64 2D transition-metal carbide (MXene) to determine that they were acceptable semiconductors for solar cells via material screening. $\text{Ti}_2\text{CO}_2/\text{Zr}_2\text{CO}_2$ and $\text{Ti}_2\text{CO}_2/\text{Hf}_2\text{CO}_2$ heterostructure solar cells, in particular, have really high power conversion efficiency of 22.74 and 19.56 percent, respectively (Most PCEs inside this paper were evaluated at AM-1.5G-illumination). This research opens the path for MXenes to be used as solar materials in the future [88]. According to Saeed et al., many new opportunities for creating effective indoor organic photovoltaics (OPVs) for practical applications can be explored. With the introduction of different optoelectronic methods to improve device performance under low indoor lighting with varied spectra, the indoor efficiency of OPVs (for PCE > 30%) has taken a quantum leap [89]. Saeed et al. demonstrated additional enhancements to dye-sensitised photovoltaic cells (DSPVs) in indoor solar applications for light energy recycling due to its outstanding light-harvesting performance under ambient lighting conditions. DSPVs' suitability for ambient energy harvesting is proven by their record high power conversion efficiency (PCE) of over 30% under indoor lighting circumstances, consistent device operation, cost-effectiveness, colorful aesthetics, and PCE retention of up to 99% [90].

3. Applications of MXene in Solar Cells

3.1. MXene as Conducting Additives in Solar Cells' Photoactive Active Layer

MXene as a photoactive layer additive in SCs is discussed in this section. Despite significant advances in PCE, charge-carrier recombination inside of the photoactive layer and at perovskite/ETL and perovskite/HTL interfaces still limits PSC performance. Improvements in charge-carrier management are essential to closing the gap between the existing PCEs and the theoretic efficiency frontier of CSs. Prior to mass manufacturing, the intrinsic instability of perovskite in humidity and at high temperatures, as well as the device's limited scalability, must be addressed. Two-dimensional nanomaterials with distinct characteristics have been investigated as additions in photoactive perovskite layers of the HTL/ETL of PSC in recent years. The use of additive engineering to enhance the surface coverage and crystallisation of perovskite films has proven to be successful.

Guo et al. investigated the inclusion of $\text{Ti}_3\text{C}_2\text{T}_x$ in the MAPbI_3 -based perovskite absorber for the first time in 2018 [77], kicking off research on MXenes in solar cells. Their findings indicate that adding $\text{Ti}_3\text{C}_2\text{T}_x$ to MAPbI_3 may prolong the nucleation process, resulting in larger crystals. Furthermore, the $\text{Ti}_3\text{C}_2\text{T}_x$ additive is extremely helpful in speeding electron transport across the grain boundary, similar to a carrier bridge [91–94]. This is measured by the reduced charge-transfer resistance for the $\text{Ti}_3\text{C}_2\text{T}_x$ additive, as revealed by the electrochemical impedance spectra. The median power conversion efficiency (PCE) rises from 15.2 percent to 16.8 percent because of these factors. In addition to adding $\text{Ti}_3\text{C}_2\text{T}_x$ to the photoactive MAPbI_3 layer, similarly, Agresti et al. added $\text{Ti}_3\text{C}_2\text{T}_x$ to the TiO_2 /ETL to fine-tune its work function (WF). This lowered it from 3.91 to 3.85 eV, which is beneficial for tuning the interfacial energy levels between the perovskite absorber and the TiO_2 /ETL, improving charge transfer and lowering the barrier height. The device achieves a PCE of 20.14 percent, which is 26.5 percent greater than the control device without the $\text{Ti}_3\text{C}_2\text{T}_x$ addition, thanks to the double addition and optimisation of both the photoactive MAPbI_3 and the TiO_2 electron transport layer. Furthermore, the inclusion of $\text{Ti}_3\text{C}_2\text{T}_x$ to the current density-voltage (JV) curves was shown to decrease hysteresis while enhancing the PSCs' long-term exposure stability. Recently, this group used density functional calculations to further investigate the MAPbI_3 perovskite/ $\text{Ti}_3\text{C}_2\text{T}_x$ -based MXene interface. When the relative concentrations of the OH, O, and F termination groups were changed, the findings indicate that the work function interface displays highly nonlinear behaviour, and they offer a profound insight into the alignment of the energy level for the manufacture of high-performance materials [15].

Agresti et al. used $\text{Ti}_3\text{C}_2\text{T}_x$ MXene in MAPbI_3 PSCs to modify the work function of perovskite films and ETLs, resulting in a power conversion efficiency improvement of 26%, as compared to $\text{Ti}_3\text{C}_2\text{T}_x$ -free control devices [95]. Di Vito and his colleagues used DFT to conduct first-principles calculations on a $\text{Ti}_3\text{C}_2/\text{MAPbI}_3$ perovskite-coupled system, linking WF tuning to changes in the various concentrations of OH-, O-, and F-MXene-Terminations, and found that OH collections had the greatest impact in reducing work function [94].

Zhang and his colleagues used an in situ solution growth technique to synthesise MAPbBr_3 nanocrystals (NCs) on the surface of multilayer MXene ($\text{Ti}_3\text{C}_2\text{T}_x$) nanosheets that form heterostructures in 2020 [96]. PSCs were manufactured utilising the C-TiO₂/m-TiO₂-TQD/TQD-Perovskite/Spiro-OMeTAD-Cu_{1.8}S design to enhance PCE and device stability while retaining a champion hysteresis-free power conversion efficiency of 21.64% compared to 18.31% for control devices, with substantially better long-term air and light stability. The entire potential of MXene materials in SCs must be explored as a new area. Various groups, on the other hand, revealed different methods for making use of 2D MXene materials' higher electrical conductivity. 2D $\text{Ti}_3\text{C}_2\text{T}_x$ MXene nanosheets were used as nanoscale additives in 2D Ruddles-den-Popper PSCs by Jin et al. The PCE of 2D PSCs rose from 13.69 percent (control device without MXene additive) to 15.71 percent [97] due to passivated trap states, optimal orientation, reduced charge transfer resistance, and enhanced crystallinity. Yang et al. utilised SnO_2 - Ti_3C_2 MXene nanocomposites as electron transport layers (ETLs) in planar PSCs [98].

Zhao et al. utilised $\text{Ti}_3\text{C}_2\text{T}_x$ MXene nanosheets as a multifunctional additive in a two-step method to create extremely efficient planar PSCs in 2021. The findings indicate that single-layer $\text{Ti}_3\text{C}_2\text{T}_x$ nanosheets improve the reactivity of the PbI_2 -layer by inducing the formation of a porous PbI_2 -layer, which increases the perovskite grain size and lowers the amount of residual PbI_2 in the perovskite film. Random stacking of large PbI_2 grains readily leads to the formation of pores, according to previous research [99]. The mechanism diagram to produce high-quality perovskite films is shown in Figure 2. $\text{Ti}_3\text{C}_2\text{T}_x$ can also improve the WF of MAPbI_3 , allowing for better energy-level alignment between the perovskite layer and the ETL. Finally, by interacting with the under-coordinated Pb^{2+} , the terminal collections on the surface of $\text{Ti}_3\text{C}_2\text{T}_x$ play a critical role in the passivation of perovskite films. The maximum PCE of 16.45 percent and a PCE rate of 15.94 percent were obtained at the optimum $\text{Ti}_3\text{C}_2\text{T}_x$ dose of 0.03 percent by weight. These values are about 18 percent better than those of pure PSCs, which had the greatest power conversion efficiency of 16.45 percent and a PCE rate of 15.94 percent. As a result, this research established $\text{Ti}_3\text{C}_2\text{T}_x$ as an effective and feasible addition for the manufacture of greatly efficient two-stage produced PSCs, paving the path for their application to other 2D materials [100].

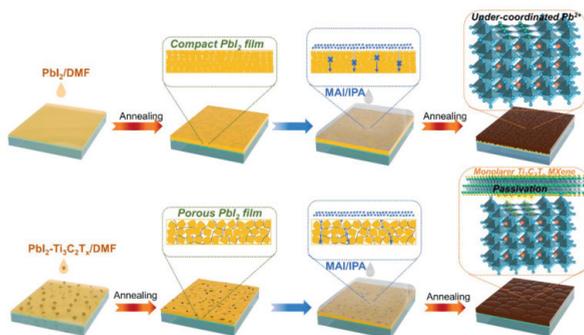


Figure 2. Mechanism diagram for the production of high-quality perovskite films processed in two steps, supported by the additive $\text{Ti}_3\text{C}_2\text{T}_x$. Reprinted with permission from ref. [100]. Copyright 2020 Elsevier B.V.

Larciprete et al. investigated pure environmental aging and the thermally driven breakdown of the mixed halide perovskite $\text{Cs}_x(\text{FA}_{0.83}\text{MA}_{0.17})(1-x)\text{Pb}_3$ using X-ray photoelectron spectroscopy ($\text{I}_{0.83}\text{Br}_{0.17}$) and high-resolution ultraviolet. The scientists also looked at the impacts of the $\text{Ti}_3\text{C}_2\text{T}_x$ MXene additive on photovoltaic stability as part of their research. Furthermore, the absence of any negative impact on PV stability, as well as a significant stabilising effect of the additional MXene, contribute to long-term aging. In the fresh samples, we observed a modest decrease in the initial halide migration rate, but this needs more investigation. In conclusion, we believe that our findings on $\text{Cs}_x(\text{FA}_{0.83}\text{MA}_{0.17})(1-x)\text{Pb}_3$ ($\text{I}_{0.83}\text{Br}_{0.17}$) show severe criticality in the stability of certain mixed perovskites that are comparable to single-halide materials. As a result, it appears that the effectiveness of agents based on electronic and chemical stabilisation of their functional properties, as well as the creative development of device architectures capable of interacting with disruptive agents, are critical for the long-term use of mixed perovskite [101].

For the first time, Hou & Yu showed further improved IPSCs using $\text{Ti}_3\text{C}_2\text{T}_x$ nanosheets as an additive in ZnO. The creation of the Zn–O–Ti bond enhances the PCE when ZnO is modified with $\text{Ti}_3\text{C}_2\text{T}_x$, because of the recently created charge transfer routes between both the passivated surface of ZnO films and the ZnO nanocrystals. Figures 3 and 4 illustrate energy level diagrams of the materials utilised in IPSCs. When compared to the control device that utilises pure ZnO as ETL, ITIC-based IPSCs with ZnO/ $\text{Ti}_3\text{C}_2\text{T}_x$ /ETL achieve an average power conversion efficiency of 12.20 percent, which is a 15.53 percent improvement (10.56 percent). PM6: Y6 IPSCs reach a champion power conversion efficiency of 16.51 percent based on the ZnO/ $\text{Ti}_3\text{C}_2\text{T}_x$ interface layer, compared to 14.99 percent for the reference device [102].

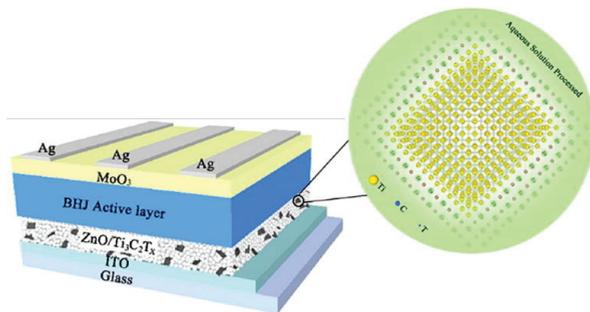


Figure 3. Schematic representation of the IPSCs configuration. Reprinted with permission from ref. [102]. Copyright 2020 Elsevier B.V.

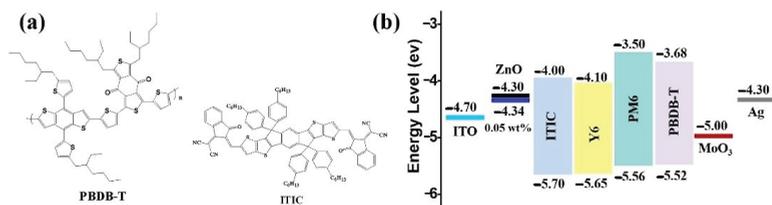


Figure 4. (a) Chemical structures of PBDB-T and ITIC. (b) Band diagram of the materials used in IPSCs. Reprinted with permission from ref. [102]. Copyright 2020 Elsevier B.V.

According to Jin et al., a modest doping level of $\text{Ti}_3\text{C}_2\text{T}_x$ nanosheets significantly enhanced the quality of 2D perovskite (BA) 2 (MA) 4 Pb_5I_{16} films and the photovoltaic performance of the associated device, with a PCE increase from 13.7 to 15.7 percent due to the increase in current. Figure 5a depicts the architecture of the current PSCs, as well as an example of $\text{Ti}_3\text{C}_2\text{T}_x$ incorporation into a 2D perovskite film. Figure 5b shows the

JV curves of the devices constructed using the control, $\text{Ti}_3\text{C}_2\text{T}_x$ 0.1 mM, $\text{Ti}_3\text{C}_2\text{T}_x$ 0.3 mM, $\text{Ti}_3\text{C}_2\text{T}_x$ 0.5 mM, and $\text{Ti}_3\text{C}_2\text{T}_x$ 0.7 mM samples. The external quantum efficiency (EQE) spectrum displayed in Figure 5c supports this growth in short-circuit current density (J_{sc}). Furthermore, a steady power output compatible with the JV curves is shown by the photocurrent evaluated for much more than 5 min at a point of maximum power (0.80 V) (Figure 5d). The enhanced vertically directed growth, uniform phase distribution in the thin film, and the crystallinity, which eventually improves charge transfer, are primarily responsible for the $\text{Ti}_3\text{C}_2\text{T}_x$ -doped components' superiority. Furthermore, owing to the superior crystallinity and passivation effect of the perovskite film, the components doped with $\text{Ti}_3\text{C}_2\text{T}_x$ nanosheets had a greater moisture stability than the shell components [99]. We can conclude that MXene has many functions in solar cells. As an additive, it accelerates electron transport by acting as an "electron" bridge. Hence, by its addition, it influences the carrier transport materials' work function and other characteristics like conductivity. This research offers a viable approach for enhancing the efficiency of 2D perovskite film and expands the scope of $\text{Ti}_3\text{C}_2\text{T}_x$'s photovoltaic applications [99].

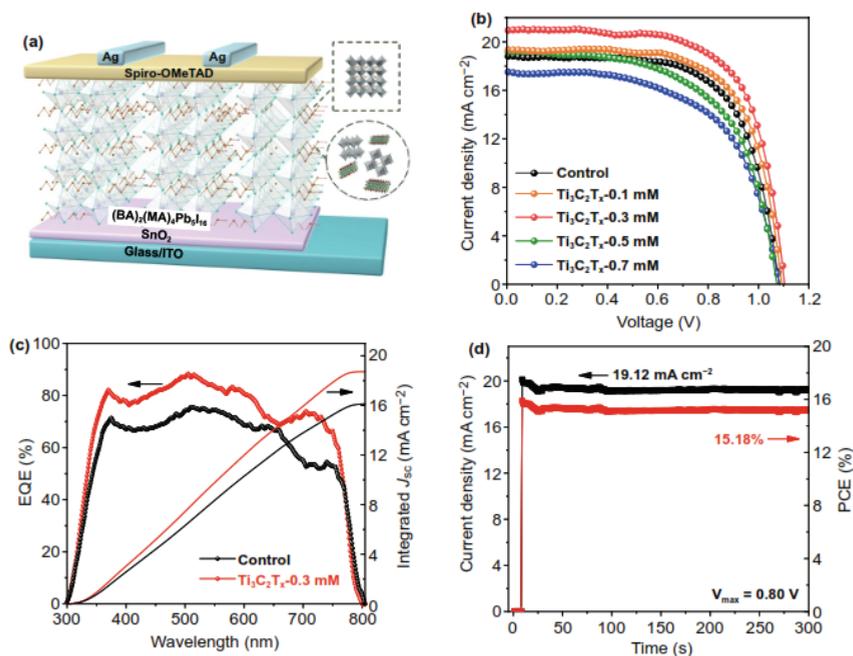


Figure 5. (a) Schematic representation of devices with the structure glass/ITO/ SnO_2 /2D perovskite/SpiroOMeTAD/Ag. (b) JV curves from devices with different amounts of $\text{Ti}_3\text{C}_2\text{T}_x$ doping. (c) EQE spectra and integrated J_{sc} of the control and optimised $\text{Ti}_3\text{C}_2\text{T}_x$ doping devices. (d) Stabilised power output and current density at a constant bias 0.80 V for the $\text{Ti}_3\text{C}_2\text{T}_x$ dopant devices. Reprinted with permission from ref. [99]. Copyright 2021 Springer Nature Switzerland AG. Part of Springer Nature.

3.2. Novel Metal Transparent Conductive Electrode

In PSCs, MXene is used as an electrode. An electrode is one of the most essential components of a PSC for controlling the charge collecting process; it is important for long-term stability and affects the device's overall cost. Metal thin-film electrodes, nanostructured metal electrodes [103], carbon electrodes [104], and graphene electrodes [105], Ref. [106] are some of the newly described electrode materials for PSC.

The $\text{Ti}_3\text{C}_2\text{T}_x$ MXene recently reported an electrical conductivity of up to $15,100 \text{ S cm}^{-1}$ [107], as well as great transparency, good flexibility, and tunable WF [108–110]. Because of these characteristics, $\text{Ti}_3\text{C}_2\text{T}_x$ may be used as an electrode in optoelectronic devices such as solar cells. The next sections elaborate on Si-wafer-based, organic, perovskite-based, and dye-sensitised solar cells, in that sequence. In quantum-dot-sensitised solar cells, the $\text{Ti}_3\text{C}_2\text{T}_x$ MXene was also utilised to make the counter electrode (CE) (QDSCs). Chen et al. described a hybrid CE made up of hydrothermally produced CuSe nanoparticles on $\text{Ti}_3\text{C}_2\text{T}_x$ -MXen nanosheets screen printed on graphite foil [111]. This composite CE offers higher electrical conductivity for electron transport and a greater specific surface area than CuSe and $\text{Ti}_3\text{C}_2\text{T}_x$ -based CEs, allowing for more active centers for polysulfide electrolyte reduction. The device can obtain a PCE of 5.12 percent by employing a CuSe- $\text{Ti}_3\text{C}_2\text{T}_x$ hybrid CE with an optimum mass ratio. Devices that utilise CuSe and $\text{Ti}_3\text{C}_2\text{T}_x$ -based CEs, on the other hand, have a PCE of 3.47 percent and 2.04 percent, respectively. Similarly, Tian et al. used a simple ion-exchange technique at ambient temperature to produce CuS/ Ti_3C_2 composite CEs, which exhibited a substantially higher electrocatalytic rate for polysulfide reduction than pure CuS [112]. The overall PCE of the QDSC based on this composite CE is 5.11 percent, which is 1.5 times higher than that of a device with pure CuS CE. The combined benefits of the Ti_3C_2 framework's high conductivity and the numerous catalytically active centers of the CuS nanoparticles are mostly responsible for the improved performance [15].

Cao et al. utilised 2D MXene material (Ti_3C_2) as a back electrode in non-precious metal PSCs and hole-transport materials in 2019 [78]. This increase in PCE was ascribed to the Ti_3C_2 electrode's superior charge extraction capacity and reduced square resistance when compared to carbon electrodes. Jiang and his colleagues recently reported that, by using a combination of one-dimensional carbon nanotubes (CNTs), two-dimensional Ti_3C_2 -MXene nanosheets, and commercial carbon paste as the electrode material in CsP-bBr₃-PSC, they were able to obtain a power conversion efficiency of 7.1% [19,113].

In dye-sensitised solar cells, the 2D-layered Ti_3C_2 counter electrode substantially surpassed V2C in 2021 when compared to the iodide redox couple. According to Xu et al., the catalytic activity of Ti_3C_2 may be enhanced by increasing the etching time suitably. A PCE of 6.2 percent was found in DSCs with a Ti_3C_2 counter electrode etched for 24 h. Furthermore, K⁺ intercalation has the potential to substantially boost Ti_3C_2 's catalytic activity, which is affected by the increased number of catalytic activity centers and the increased interlayer spacing for smooth iodide electrolyte transport. The PCE of the DSCs with the K⁺- Ti_3C_2 counter electrode was 7.11 percent, which was notably similar to the PCE of the conventional DSCs using Pt counter electrodes (7.2%) [114]. Chen et al. made the first effort to utilise MXene/CoS as an electrocatalytic CE for QDSSCs in their research. When compared to QDSSCs with bare MXene (4.25%) and bare CoS (5.77%) CEs, the QDSSCs with an MXene/CoS/CE exhibit a substantial improvement in cell performance and provide a promising PCE of 8.1% [115].

Additionally, a fan was installed to aid in the construction of flexible OSCs. This study emphasises the significance of developing FTEs and demonstrates their essential importance in flexible OSCs. With a sheet resistance of 110 sq^{-1} , the transparent $\text{Ti}_3\text{C}_2\text{T}_x$ MXene electrodes have the lowest sheet resistance to date. As a result, scientists and engineers should collaborate to develop FTEs with the high electrical and optical compromise needed for highly efficient flexible OSCs. Tang et al. [116] demonstrated a flexible non-fullerene OSC with Ag NW/Mxene component electrodes and PBDB-T:ITIC:PC71BM active layers utilising the Ag NW/Mxene component electrodes (Figure 6) [117].

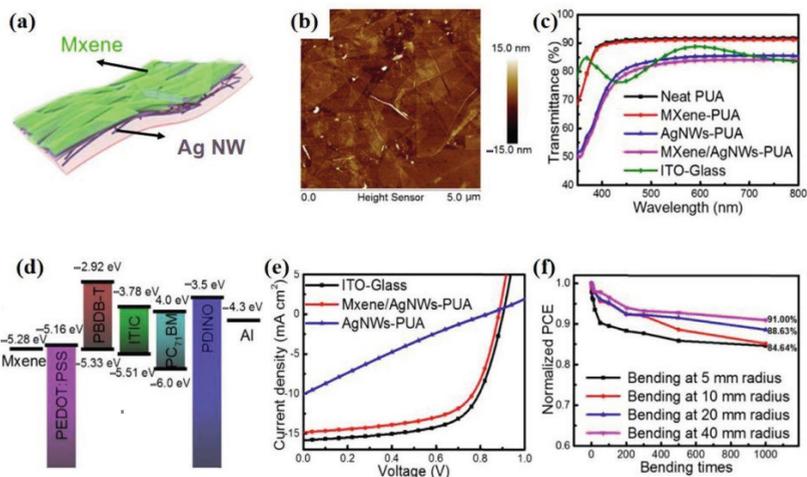


Figure 6. (a) Schematic representation of the MXene/AgNW hybrid electrodes on PUA substrates. (b) AFM images of the MXene/AgNW PUA films. (c) Transmission spectra of pure PUA, MXene-PUA, Ag NW-PUA, optimised MXene/Ag NW-PUA, and ITO glass. (d) Energy level diagrams of the flexible OSCs. (e) JV curves of the flexible OSCs with PBDB-T: ITIC: PC71BM active layers. (f) Normalised PCE of the flexible OSCs with MXene/Ag NW electrodes as a function of the number of bending cycles. Reproduced with permission. Reprinted with permission from ref. [116,117]. Copyright 2019 American Chemical Society.

Ahmed et al. studied the application of single-layer delaminated 2-D-MXene (Ti_3C_2) created by the leaching method to replace both TCO and Pt as a conductive layer and a catalyst. Each test required at least five samples. To prevent human error and obtain the greatest possible conversion efficiency for reliable comparisons, a pre-built TCO Pt meter was utilised as the reference counter electrode (CE). Figure 7 depicts the whole procedure. Furthermore, Ti_3C_2 was adjusted in thickness for optimum conversion efficiency. At optimum thickness, the TCO/Pt/free MXen-based CE had a PCE of 8.68%, which was 4.03% higher than the conventional TCO/Pt-based counter electrode. The high efficiency is attributable to the high conductivity, the large number of accessible catalytic centers owing to the delaminated structure, and Ti_3C_2 's excellent catalytic activity towards iodide and triiodide electrolytes [118].

Hence, we can conclude that MXene serves a variety of roles in solar cells. As an electrode, it improves the form of hybrid electrodes with other conducting nanomaterials, such as metallic nanowires or carbon nanotubes. In addition, it enhances transparency, increases flexibility, metallic conductivity, and influences the work functions.

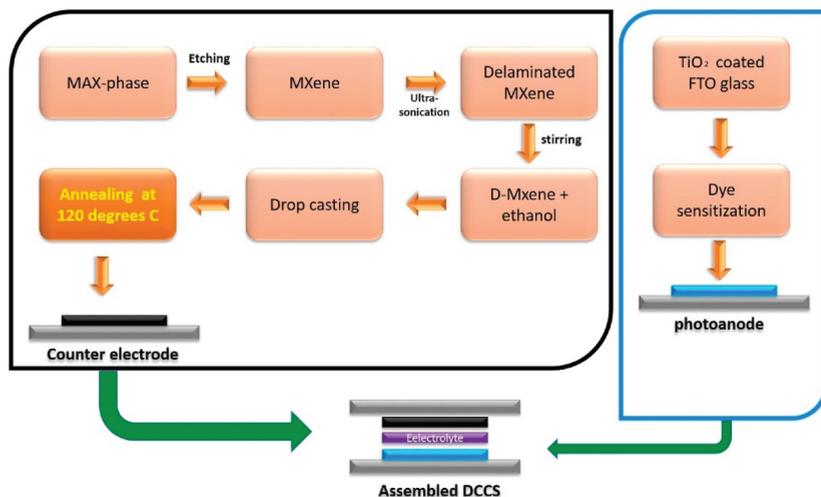


Figure 7. Schematic representation of an experimental procedure. Reprinted with permission from ref. [118]. Copyright 2021 Elsevier Ltd. and Techna Group S.r.l.

3.3. Mxene as Transfer Layer HTL/ETL in Solar Cells

The Electron Transport Layer (ETL) and Hole Transport Layer (HTL) in perovskite solar cells play an essential role in increasing stability (PSCs) and photovoltaic performance. The ETL's primary function is to collect and transmit electrons from the perovskite layer while also preventing hole backflow, efficiently segregating charges, and reducing charge recombination [119]. The HTL's primary function is to collect and transport holes from the photoactive perovskite layer to the electrode while also acting as an energy barrier to inhibit electron transmission to the anode. Furthermore, the HTL efficiently divides the photoactive perovskite layer from the anode and isolates air moisture, which enhances the stability of PSCs by reducing deterioration and corrosion [120]. The HTL PSC performance of component prototypes with various $\text{Mo}_2\text{C} @ \text{CNT}$ nanocomposite loading (1, 1.5, and 2 wt.-%) was also investigated. Then, the $\text{Mo}_2\text{C} @ \text{CNT} @ \text{PEDOT} : \text{PSS}$ HTL-based device was utilised as an X-ray photodetector, with a maximum sensitivity of 3.56 mA/Gycm². Figure 8a depicts the schematic structure of the ITO/HTL/ $\text{CH}_3\text{NH}_3\text{PbI}_3$ /ETL/LiF/Al-PSC using $\text{Mo}_2\text{C} @ \text{CNT} @ \text{PEDOT} : \text{PSS}$ as HTL in the ITO/HTL/ $\text{CH}_3\text{NH}_3\text{PbI}_3$ /ETL/LiF/Al-PSC using $\text{Mo}_2\text{C} @ \text{CNT} @ \text{PEDOT} : \text{PSS}$ as HTL. The architecture of this composite perovskite solar cell was studied using cross-sectional FESEM (Figure 8b), and the associated energy level diagram is presented in Figure 8c. The findings show that Mxene/CNT nanocomposites with a perovskite layer have the potential to improve the efficiency of SCs and photodetectors. A high PCE of 11.98 percent was obtained for the HTL containing 1.5 percent by weight $\text{Mo}_2\text{C} @ \text{CNT}$ s mixed with PEDOT : PSS in a component architecture of ITO/HTL/ $\text{CH}_3\text{NH}_3\text{PbI}_3$ /PCBM/LiF/Al, which is greater than the HTLs with Mo_2C (9.82%) and CNT (10.61%) mix [121].

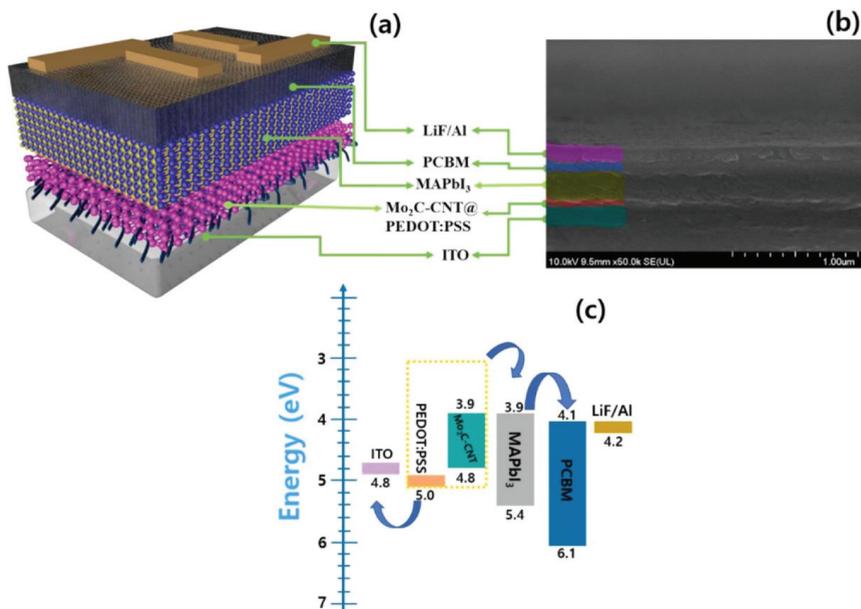


Figure 8. (a) Device architecture of the prepared ITO/HTL/ $\text{CH}_3\text{NH}_3\text{PbI}_3$ /PCBM/LiF/Al prototype using Mo_2C -CNTs @ PEDOT: PSS HTL and (b) FESEM cross-sectional image; (c) Energy level diagram for ITO/ Mo_2C -CNTs @ PEDOT: PSS/ $\text{CH}_3\text{NH}_3\text{PbI}_3$ /PCBM/LiF/Al structure. Reprinted with permission from ref. [121]. Copyright 2021 Elsevier B.V.

According to Bati et al., the incorporation of 2D MXenes into the ETL of PSCs produces extremely effective photovoltaic (PV) components. A power conversion efficiency of over 21% is obtained with the optimum composition [122]. In a planar PSC with a regular structure, Zheng et al. examined a hybrid film of SnO_2 nanoparticles and $\text{Ti}_3\text{C}_2\text{T}_x$ MXene nanoflakes as an electron transport layer (ETL). The ETL and perovskite layer production procedures are shown in Figure 9. The results show that the film qualities of the upper perovskite layers can be controlled by changing the $\text{Ti}_3\text{C}_2\text{T}_x$ / SnO_2 ratios (2.02 wt percent in ETLs), such as crystallinity, crystal size, compactness, defect density, optical absorption, surface roughness, and so on, by changing the $\text{Ti}_3\text{C}_2\text{T}_x$ / SnO_2 ratios (2.02 wt percent in ETLs) [123].

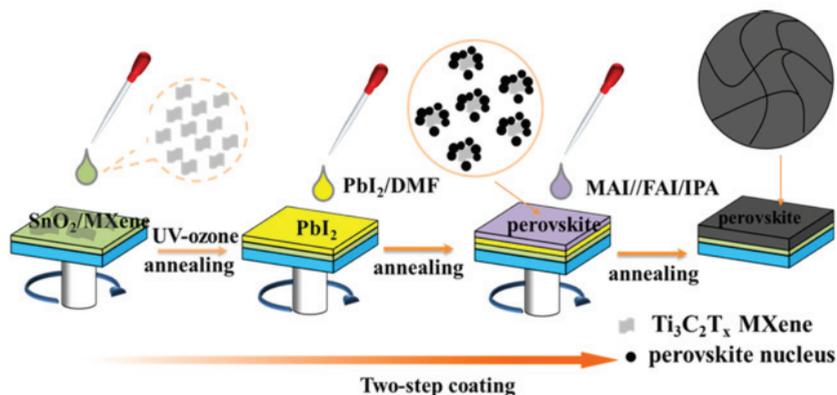


Figure 9. Schematic representation of the manufacturing processes of the perovskite film and the ETL. Reprinted with permission from ref. [123]. Copyright 2021 American Chemical Society.

J. Zhang et al. developed the Nb_2CT_x -MXene, which has outstanding photoelectric characteristics and can be utilised as the HTL in fabricating the inverted PVSCs. Enhancing the O-terminated functional groups on the Nb_2CT_x surface, oxygen plasma treatment altered the work function (WF) of Nb_2CT_x HTL. PVSCs with oxygen-plasma-treated Nb_2CT_x HTL have the greatest PCE of 20.74 percent and excellent stability. Figure 10 shows a schematic representation of the device construction as well as the structure of Nb_2CT_x MXene, as seen in Figure 10a. The PVSCs' current density–voltage curves (JV) are presented in Figure 10b for various scan directions. As demonstrated in Figure 10, the enhanced J_{sc} is attributed to the greater external quantum efficiency values (EQE) owing to more effective charge separation and collecting efficiency (Figure 10c). The Nb_2CT_x -HTL treated with oxygen plasma similarly produces flexible and large-area (0.99 cm^2) PVSCs with PCE of 17.26 percent and 17.94 percent (Figure 10d,e). Furthermore, employing Nb_2CT_x treated with oxygen plasma as HTL, the flexible and large-area (0.99 cm^2) PVSCs obtain the greatest PCE of 17.26 percent and 17.94 percent, respectively [124].

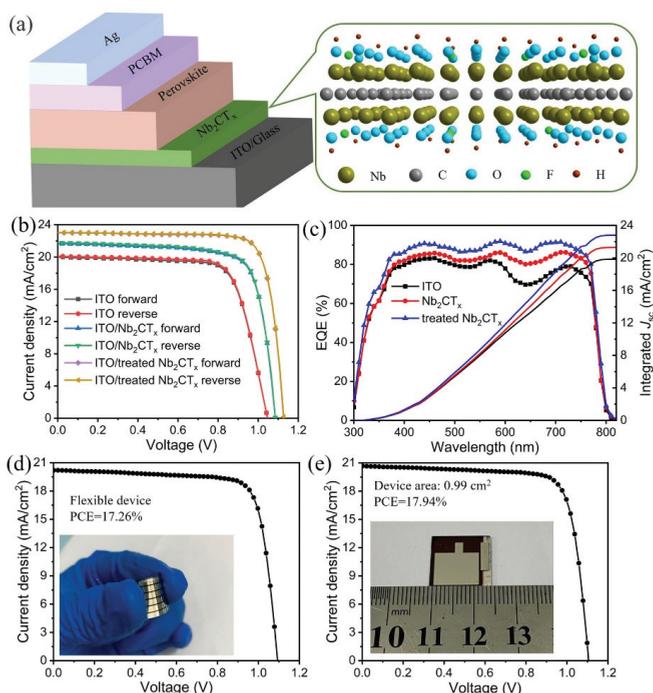


Figure 10. (a) The schematic diagram of the device structure and the structure of Nb_2CT_x MXene. (b) JV curves of PVSCs measured under different scan directions. (c) External quantum efficiency (EQE) and integrated J_{sc} curves of various PVSCs. JV curves of the flexible (d) and large-area (e) PVSCs using Nb_2CT_x -HTL treated with oxygen plasma. Reprinted with permission from ref. [124]. Copyright 2021 AIP Publishing LLC.

Wang et al. used a solution procedure at room temperature to show the potential of $\text{Ti}_3\text{C}_2\text{T}_x$ MXene as an ETL for efficient PSCs with traditional design. The authors modified the MXene surface using an oxygen plasma treatment and attempted to establish a link between the surface characteristics and MXene termination groups. The contact angle and topography measurements were used to study the surface tension of MXene and the morphology of the associated perovskite. The PbO interactions between perovskite and MXene were shown by high-resolution XPS spectra, which improved device stability [125].

Yang et al. found a superior match in energy levels between the ETL layer and the perovskite in the case of a hybrid of oxidised and pure $\text{Ti}_3\text{C}_2\text{T}_x$, with a champion PCE of 18.29 percent, compared to PSCs with pure $\text{Ti}_3\text{C}_2\text{T}_x$ as ETL, with a PCE of 16.50 percent. The intersection of the baseline with the tangent line of the spectra determined the highest occupied molecular orbital (HOMO) and the highest energy levels, while the results of the UV-Vis absorption spectra calculated the lowest unoccupied molecular orbital (LUMO). The enhanced electron mobility in the ETL, which increases electron transport and decreases hole–electron recombination, is responsible for the improvement in PCE. This research shows that these materials have a lot of promise for use in low-temperature-produced PSC and other solar technologies [126].

To develop a new $\text{ZnO}/\text{Ti}_3\text{C}_2\text{T}_x$ nanohybrid composite film, Hou & Yu utilised $\text{Ti}_3\text{C}_2\text{T}_x$, a representative of MXene, as an additive in zinc oxide (ZnO). By establishing the Zn–O–Ti bond on the ZnO surface, $\text{Ti}_3\text{C}_2\text{T}_x$ nanosheets generate new electron transport routes between ZnO nanocrystals and passivates the ZnO surface. As a consequence, the PBDB-T: ITIC based photovoltaic devices with $\text{ZnO}/\text{Ti}_3\text{C}_2\text{T}_x$ ETLs have a power conversion efficiency of 12.20 percent, compared to 10.6 percent for the comparable device utilising pure ZnO as the ETL, which is a 15.53 percent improvement. Furthermore, PM6: Y6-based IPSCs obtain a champion power conversion efficiency of 16.5 percent, compared to 15 percent for the reference device, demonstrating the $\text{ZnO}/\text{Ti}_3\text{C}_2\text{T}_x$ —ETL's applicability [102]. Saranin et al. showed that by utilising MXenes as doping for the forming layers, it is possible to adjust the optoelectronic characteristics of inverted p-i-n-perovskite components. When compared to reference cells, the MXene-based devices had a maximum PCE of over 19% and an average growth of +8%, which is a surprising result, given that the MAPbI₃-based p-i-n cell used spin-coated NiO [127].

4. Conclusions and Prospect

From the discovery of MXene in 2011 up to now, MXene has achieved tremendous technological developments. In 2018, MXene entered into the development of solar cell production by enhancing the effectiveness of energy produced and the stability of solar cells. This review attempts to compile all previously published research on adding MXene into PSCs to enhance operational stability and solar energy collection. According to MXene's function, the most essential device parameters are given in Tables S1–S3 (Supplementary Materials).

The main conclusions of this work are:

1. Adoption of perovskite solar cells for effective use in solar energy technology due to their good stability against moisture, heat, and light as well as good crystallisation and low density of defects in perovskite films.
2. The use of titanium carbide ($\text{Ti}_3\text{C}_2\text{T}_x$) in perovskite solar cells resulted in a steady-state energy conversion efficiency of 23.3% and outstanding stability.
3. MXenes combine with other materials to create hybrids and nanocomposites with improved or additional functions. These innovative materials could be used in applications such as renewable energy, energy storage, and conversion.
4. It has become clear to us that the use of a hybrid MXene with carbon nanotubes (m-SWCNTs) can effectively improve the photovoltaic performance of perovskite solar cells due to the presence of hybrid interfacial layers that can reduce defect density and thus improve charge extraction and transfer.
5. From the above tables, it is clear to us that in the last year, the use of MXene as an electron transport layer (ETL) for solar cells has dominated scientific research due to efficient PSCs with conventional design through a solution method at room temperature.
6. All kinds of 2D transition-metal MXenes demonstrated behavior not previously seen in mono-M MXenes, indicating the potential for the use of 2D transition-metal MXenes in a variety of novel applications. Researchers can tune the performance of MXenes for a variety of applications, including nanomagnets, transparent electronics,

semiconductors, supercapacitors, and structural materials, by controlling the composition of the 2D transition-metal MXenes phase. This level of control over their composition and structure is unique in the area of 2D materials, and it opens up new avenues for nanomaterial design. The addition of 2D transition-metal MXenes to the category of 2D materials has increased the design options for nanomaterials to satisfy the needs of growing technology.

Supplementary Materials: The following are available online at <https://www.mdpi.com/article/10.3390/nano11102732/s1>, Tables S1–S3: Summary of the key parameters for the solar cells employing MXenes.

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Conflicts of Interest: The authors declare no conflict of interest.

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Article

Nanostructured Molybdenum-Oxide Anodes for Lithium-Ion Batteries: An Outstanding Increase in Capacity

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Abstract: This work aimed at synthesizing MoO₃ and MoO₂ by a facile and cost-effective method using extract of orange peel as a biological chelating and reducing agent for ammonium molybdate. Calcination of the precursor in air at 450 °C yielded the stoichiometric MoO₃ phase, while calcination in vacuum produced the reduced form MoO₂ as evidenced by X-ray powder diffraction, Raman scattering spectroscopy, and X-ray photoelectron spectroscopy results. Scanning and transmission electron microscopy images showed different morphologies and sizes of MoO_x particles. MoO₃ formed platelet particles that were larger than those observed for MoO₂. MoO₃ showed stable thermal behavior until approximately 800 °C, whereas MoO₂ showed weight gain at approximately 400 °C due to the fact of re-oxidation and oxygen uptake and, hence, conversion to stoichiometric MoO₃. Electrochemically, traditional performance was observed for MoO₃, which exhibited a high initial capacity with steady and continuous capacity fading upon cycling. On the contrary, MoO₂ showed completely different electrochemical behavior with less initial capacity but an outstanding increase in capacity upon cycling, which reached 1600 mAh g⁻¹ after 800 cycles. This outstanding electrochemical performance of MoO₂ may be attributed to its higher surface area and better electrical conductivity as observed in surface area and impedance investigations.

Keywords: molybdenum oxides; green synthesis; biological chelator; additional capacity; anodes; lithium-ion batteries

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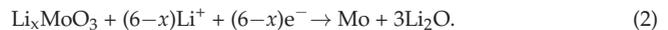
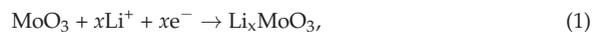
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1. Introduction

Understanding and realization of the benefit of efficient energy storage is one of the most important strategies for achieving sustainable development [1,2]. Nowadays, lithium-ion batteries (LIBs) have become one of the most important energy storage technologies due to the fact of their higher storage capacity and power density compared to other rechargeable batteries [3–5]. The development and rapid increase in portable electronic devices and electric vehicles have accelerated the pursuit of developing LIBs with high energy and power densities [6,7]. Therefore, it is essential to develop high-capacity electrode materials for LIBs [8–13]. Graphite has become the standard anode material for LIBs since their commercialization by Sony Corporation [14]. However, graphite has relatively low theoretical capacity (372 mAh g⁻¹ and 850 mAh cm⁻³), which cannot meet the demand of current large-scale energy applications [15]. To address this issue, there is a continuous

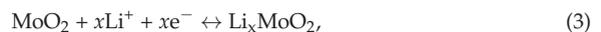
effort to explore alternative anode materials. For instance, transition metal oxides (TMOs), such as NiO, MnO₂, TiO₂, Fe₃O₄, MoO₃, and MoO₂, have been studied as anode materials for LIBs. These oxides are abundant, low cost, and have a high theoretical specific capacity of approximately 500–1200 mAh g⁻¹ due to the fact of their conversion reaction upon lithiation [16–21].

Molybdenum oxides with different oxidation states (e.g., MoO₃, MoO_{3-δ}, Mo_nO_{3n-1}, and MoO₂) and a broad spectrum of electrical properties ranging from wide band gap semiconducting (MoO₃) to metallic (MoO₂) character are considered as promising anode materials for LIBs [22]. Their specific capacities are significantly higher than that of graphite [23–29]. In particular, MoO₃ with an orthorhombic crystal structure is a thermal stable, abundant, cost effective, and a rather safe oxide with a theoretical capacity of 1117 mAh g⁻¹ and a typical discharge potential plateau around 0.45 V [30–34]. It has a unique layered structure that is convenient for fast lithium diffusion transport [15,35–38]. The overall first lithiation reaction for MoO₃ is described by two reactions: the lithium insertion (addition) at a potential >1.5 V up to $x \approx 1.2$ (Equation (1)) and the conversion (transformation) reaction at a potential <0.5 V up to $x \approx 6.0$ (Equation (2)) as follows [22]:



Some drawbacks have been reported for MoO₃, such as phase transformation accompanied by volume expansion with repeating cycling, which leads to a rapid capacity fading [39,40].

On the other hand, MoO₂ crystallizes in the monoclinic structure with space group $P2_1/c$, which can be viewed as a distorted rutile phase. This structure is composed of MoO₆ octahedra joined by edge-sharing, which form a (1 × 1)-tunneling network [41,42]. In addition, MoO₂ has outstanding properties for energy storage applications, e.g., metal-like conductivity ($\sim 6 \times 10^3 \text{ S cm}^{-1}$), very low toxicity, cost-effectiveness, high chemical and thermal stability, high volumetric capacity due to the fact of its high density (6.5 g cm⁻³), and high theoretical capacity (838 mAh g⁻¹) [43–45]. The first lithiation mechanism is an insertion-type reaction that takes place in the bulk and amorphous MoO₂ electrodes with only one-electron reduction as described by Equation (3) [46]:



with $0 \leq x \leq 0.98$. The second mechanism is a conversion reaction that gradually resolves Li_xMoO₂ as described by Equation (4) [47]:



that shows the formation of metallic Mo and Li₂O.

MoO₃ and MoO₂ have been prepared in different morphologies, e.g., nanoparticles [48], nanowires [49,50], nanorods [51,52], nanotubes [53], nanosheets [54], and nanobelts [55]. These nanosized fabrications were expected to improve the electrochemical performance [56]. However, these fabrication methods are complicated, expensive, energy- and time-consuming, and non-scalable [57]. To alleviate these limitations, to some extent, an attempt was made to use a rather benign approach via simple, green, and eco-friendly reducing agents for nanoparticles formation [58]. Green synthesized particles have low toxicity and are more stable than those prepared by traditional methods, as biological sources provide a stabilizing and capping effect for the synthesized particles, especially extracts of plants [58].

Extracts of waste products have been used as cost-effective, eco-friendly, and efficient raw materials for various energy storage applications [59,60]. In our previous work, we used extracts of lemon and orange peels to synthesize manganese dioxides, which has been used as cathode materials in LIBs and supercapacitors [60,61]. Further processing and using large quantities of orange peels as a byproduct will reduce hazardous impacts and

serious environmental pollution [60]. Orange peels contain polyphenolic and flavonoid compounds which have hesperidin, narirutin, naringin, and eriocitrin [62]. It is well known that the phenolic compounds have at least one aromatic ring. The latter is attached to one or more hydroxyl groups. The number and position of the carboxylic group has a direct impact on reducing the antioxidant ability of flavonoids and phenolic acids. As the number of hydroxyl group increases, the antioxidant activity increases [63]. Orange is considered as one of the most important fruits with a global production of 48.8 (2016/17) million tons. Industrial extraction of citrus juice consumed a large portion of this production. As a result of this industry, there are large amounts of residues, e.g., peel and segment membranes. A high percent of these residues is related to peel byproduct that represents between 50% and 65% of the total weight of the fruit; reported chemical analysis for orange peel showed 7.1% protein and 12.79% crude fiber. In addition, limonoids and flavonoids with antioxidant activity were also found in orange peel. This antioxidant activity of citrus peel extracts comes from glycosides hesperidin and naringin present in this extract. Orange peel also contains coniferin and phlorin as additional phenols that help in radical scavenging when administered in the form of orange peel molasses, and this will promote sustainable disposal of orange peels [64].

In this study, orange peel extract was used as an effective chelating agent to synthesize molybdenum oxides. MoO_3 and MoO_2 were prepared by altering the calcination conditions: in air for MoO_3 and in vacuum for MoO_2 at a low temperature of 450 °C. The as-prepared oxides were subjected to various characterizations, including X-ray diffraction (XRD), thermogravimetric analysis (TGA), scanning electron microscopy (SEM), transmission electron microscopy (TEM), Raman scattering (RS) spectroscopy, and X-ray photoelectron spectroscopy (XPS), to elucidate their morphological and structural properties. Further electrical and electrochemical characterizations, including cyclic voltammetry (CV), galvanostatic charge–discharge (GCD), electrochemical impedance spectroscopy (EIS), and area-specific impedance (ASI), were carried out for the as-prepared molybdenum oxides as anode materials for LIBs.

2. Materials and Methods

Ammonium molybdate, conductive carbon black super C65 (Timcal Co., Bodio, Switzerland), binder polyvinylidene fluoride (PVDF, 12 wt.%, Kureha Battery Materials Japan Co., Tokyo, Japan), solvent 1-methyl-2-pyrrolidinone (NMP, anhydrous 99.5%, Sigma–Aldrich, Burlington, MA, USA), electrolyte 1 mol L^{−1} LiPF₆ in ethylene and dimethyl carbonate solution mixed as a 1:1 volume ratio (BASF Corporation, Ludwigshafen-am-Rhein, Germany), and lithium ribbon (thickness 0.38 mm, 99.9% trace metals basis, Sigma–Aldrich, Burlington, MA, USA) were employed as received.

Molybdenum oxides were prepared by the sol-gel method using ammonium molybdate tetrahydrate, $(\text{NH}_4)_6\text{Mo}_7\text{O}_{24}\cdot 4\text{H}_2\text{O}$ as the source of molybdenum, and extract of orange peel as the chelating agent. Pure filtrated extract of orange peel was obtained through boiling small pieces of cleaned waste peels in distilled water at 100 °C for 10 min. A schematic representation of the MoO_3 and MoO_2 growth process is shown in Figure 1. Pure orange peel extract drops were added with vigorous stirring to a 100 mL solution of 4 g of $(\text{NH}_4)_6\text{Mo}_7\text{O}_{24}\cdot 4\text{H}_2\text{O}$. During this operation, the solution changed in color from yellow to blue until conversion to a dark gel. The dry xerogel (precursor) was divided into two parts: one part was calcined in air at 450 °C for 5 h (MOA, yellow color) and the second was calcined under vacuum at 450 °C for 5 h (MOV, black color).



Figure 1. Schematic diagram for the synthesis of MoO_3 (yellow color) and MoO_2 (black).

XRD analyses of as-prepared samples were processed using a Bruker D8 Discover XRD Instrument equipped with $\text{CuK}\alpha$ radiation ($\lambda = 1.5406 \text{ \AA}$). The scanning rate was $1.2^\circ \text{ min}^{-1}$, for 2θ between 10° and 80° . Raman spectra were recorded at room temperature with a micro-Raman spectrometer (Renishaw, Wotton-under-Edge, UK) with a confocal Raman microscope inViaTM system at a 532 nm laser-line excitation. The spectra were calibrated with the reference Si phonon peak at 520 cm^{-1} . The morphology of the materials was studied by field emission scanning electron microscopy (FESEM, JEOL JSM-7800F) and by transmission electron microscopy (TEM, JEOL, JEM-2100 microscope, Japan). BET surface area and pore size distribution of synthesized samples were determined from an N_2 -physisorption analyzer (ASAP 2020 system, Micromeritics Corporate, Norcross, GA, USA). The BET surface area was calculated from the isotherms in the range from 0.02 to 0.4 of relative pressures (P/P_0). TGA measurements were carried out for the prepared samples using a thermal gravimetric analyzer (Perkin Elmer, TGA 7 series) in a temperature range of $50\text{--}1000^\circ \text{C}$ at a heating rate of $10^\circ \text{C min}^{-1}$ in air. X-ray photoelectron spectra were recorded using a PHI VersaProbe II Scanning X-Ray Microprobe system equipped with a Mg $\text{K}\alpha$ source ($\lambda = 1253.6 \text{ eV}$).

LIB electrodes were fabricated as a mixture of active materials (Mo oxide powders), carbon black (CB), and polyvinylidene fluoride binder (PVDF) in a 5:3:2 mass ratio. We used a high percentage of carbon black and PVDF binder in the electrode to maintain the mechanical integrity and good electrical connection in the electrode during long-term cycling experiment. The mixture was added to N-methyl-2-pyrrolidone (NMP) solvent. The mixed slurry was magnetically stirred for 24 h to form a homogeneous blend. The well-blended slurry was cast on a copper foil by a doctor blade and was dried under vacuum at 100°C for 24 h. Finally, electrodes were punched out as $\sim 0.97 \text{ cm}^2$ discs ($\Phi = 11 \text{ mm}$). CR2032 coin cells processed in an argon-filled glovebox using $30 \mu\text{L}$ electrolyte dripped on the electrode, then on a Celgard 2400 separator. Electrochemical tests were carried out using an Arbin BT2000 battery cyler at room temperature. Before cycling, cells were initially maintained at rest for 30 min. Cells were cycled galvanostatically at C/10 and 1C-rate ($1\text{C} = 838 \text{ mA g}^{-1}$ for MoO_2 and $1\text{C} = 1117 \text{ mA g}^{-1}$ for MoO_3) in a voltage range between 0.01 and 3.0 V. Cyclic voltammetry was conducted at room temperature on a BioLogic VSP workstation in which the potential was set to sweep from open-circuit voltage to 0.01 V and then to sweep back to 3.0 V at a 0.02 mV s^{-1} scanning rate. Electrochemical impedance spectroscopy was also conducted by the VSP workstation in the frequency range from 5×10^5 to 0.1 Hz with an amplitude of 5 mV.

3. Results

3.1. Structure and Morphology

The X-ray diffractograms of MOA and MOV materials are shown in Figure 2a. Patterns display well-resolved reflections with a very smooth background indicating the high crystallinity of Mo oxides prepared by the sol-gel method with biological chelating agent and final calcination at 450°C . The XRD spectrum of MOA exhibited the typical pattern of the $\alpha\text{-MoO}_3$ phase and can be indexed in the orthorhombic structure with $Pbnm$ space

group (JPCDS card 76-1003) [65]. The presence of a preferred orientation of (0*k*0) planes was evidenced by the (020), (040), and (060) Bragg lines with large intensities. The XRD spectrum of the MOV material displayed sharp diffraction peaks indicating the formation of highly crystallized MoO₂, which can be indexed using the monoclinic structure with the *P*2₁/*c* space group (JPCDS card 68-0135). In order to characterize the phase purity as well as the phase composition, the full structural identification of the MoO₃ and the MoO₂ powders were analyzed using Rietveld refinements. The results are listed in Table 1, and the refined XRD spectra are displayed in Figure 2b,c. The small values of the residual and reliability parameters (*R*_p, *R*_w, and χ^2) of the Rietveld refinement indicate the successful identification of the orthorhombic and monoclinic phases of MoO₃ and MoO₂ powders, respectively, even in the presence of some impurity phases as in the case of MOV. The lattice parameters obtained from Rietveld refinement are in good agreement with values of our previous work as well as other literature [22,66–68]. A careful examination of the MoO₂ sample calcinated in vacuum reveals the presence of a small amount of Mo-suboxides such as Mo₄O₁₁, Mo₈O₂₃, and Mo₉O₂₆ (Table 1). These compositions belong to Mo_{*n*}O_{3*n*-1} suboxides (Magnéli phases, *n* = 4–9), which crystallize into the ReO₃-type structure characterized by the presence of empty channels due to the loss of oxygen [23,68,69]. These compositions (Mo₄O₁₁, Mo₈O₂₃, and Mo₉O₂₆) deduced from Rietveld refinement imply the presence of a mixture of Mo with oxidation states between +6 and +4. This electronic configuration implies a concentration of free carriers and, thus, a large electrical conductivity, which is beneficial to electrochemical properties [68].

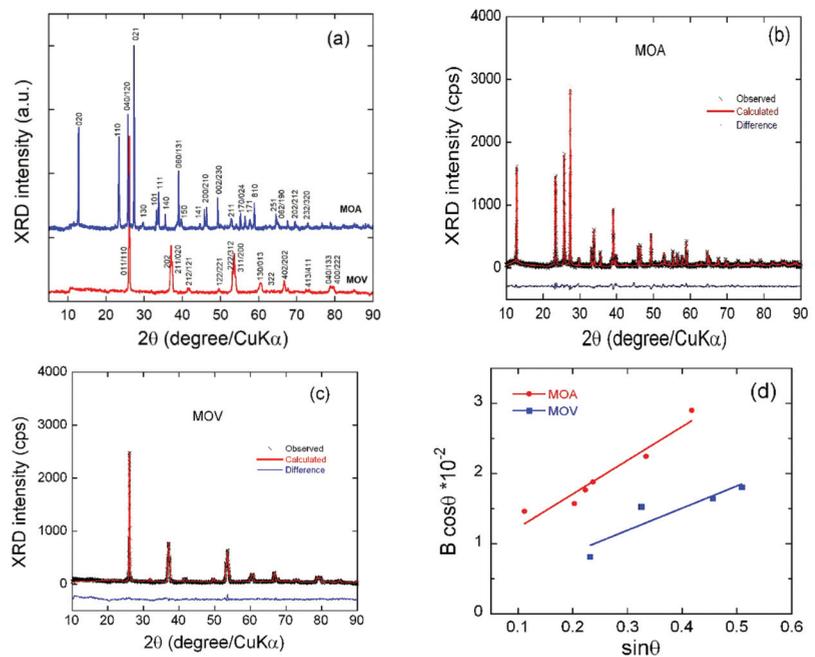


Figure 2. (a) XRD patterns of the as-prepared MOA and MOV samples. (b) Rietveld refinement of the MOA sample. (c) Rietveld refinement of the MOV sample. Cross marks are experimental data and solid lines (in red) are calculated diagrams. The curve at the bottom is the difference between the calculated and observed intensities. (d) Analysis of micro-strain from the full-width *B* at half-maximum of the XRD peaks according to Equation (1).

Table 1. Results of the Rietveld refinements for the MOA and MOV samples.

Crystal data	MOA	MOV
<i>Lattice parameters</i>		
<i>a</i> (Å)	3.69(5)	5.61(3)
<i>b</i> (Å)	13.84(8)	4.85(3)
<i>c</i> (Å)	3.95(9)	5.62(1)
<i>V</i> (Å ³)	202.6	131.3
<i>L_c</i> (nm)	29.5	45.6
$\epsilon \times 10^{-2}$ (rd)	11.9	7.9
<i>Reliability factors</i>		
<i>R_p</i> (%)	10.9	8.1
<i>R_{wp}</i> (%)	16	11.2
<i>R_{exp}</i>	9.1	7.7
χ^2	3.1	2.1
<i>Materials fraction (mol%)</i>		
MoO ₃	100	0
MoO ₂	0	90.2
Mo ₄ O ₁₁	0	2.2
Mo ₈ O ₂₃	0	4.5
Mo ₉ O ₂₆	0	3.1

The formation of Mo₄O₁₁, Mo₈O₂₃, and Mo₉O₂₆ suboxides under vacuum is due to the presence of not only the ammonia in ammonium molybdate but also the CO and CO₂ gases generated by the combustion reaction of carbon found in the organic components of orange peel (i.e., ascorbic and citric acid) which reduce the Mo⁶⁺ ions in absence of O₂. The average crystalline sizes of the prepared samples were calculated using the Debye–Scherrer’s formula from the full-width of diffraction peaks. They were found to be ≈29 and 45 nm for MOA and MOV, respectively. Further information on the structural properties can be obtained from the broadening of diffraction peaks that is considered an indicator, not only of the crystallinity of the MOA and MOV powder, but also of the homogeneous distribution of cations over the structure. The micro-strain (ϵ) of the MOA and MOV particles was determined using the Williamson–Hall equation [70]:

$$B_{hkl} \cos \theta_{hkl} = (K\lambda/L_c) + 4\epsilon \sin \theta_{hkl} \quad (5)$$

where B_{hkl} is the line broadening of a Bragg reflection (hkl), K is the shape factor, L_c is the effective crystallite size, and λ is the X-ray wavelength. The micro-strain is estimated from the slope of the plot ($B_{hkl} \cos \theta_{hkl}$) vs. ($\sin \theta_{hkl}$) and the intersection with the vertical axis provides the crystallite size. The B_{hkl} value used here was the instrumentally corrected one. From Figure 2d, the micro-strain was determined to be 11.9×10^{-2} and 7.9×10^{-2} rd for MOA and MOV, respectively, showing a slight difference in the crystallinity of the samples, as the micro-strain was strongly affected by the heat-treatment conditions.

Figure 3 displays the thermogravimetry (TG) curves of MOA and MOV samples recorded at a heating rate of $10^\circ\text{C min}^{-1}$. The MOA sample showed a stable, flat, and straight-line TG profile without weight change until the start of decomposition above 730°C . These features indicate a stoichiometric MoO₃ material without any oxygen vacancies or carbon coating due to the burning of the extract of organic peel. On the contrary, the thermal behavior of reduced MOV looked different. The TG curve was stable and flat until approximately 400°C . Above 400°C , a gradual and pronounced weight gain occurred until reaching the highest value of 10.4% weight gain, which was due to the re-oxidation and filling of oxygen vacancies in the suboxide (Mo₄O₁₁, Mo₈O₂₃, and Mo₉O₂₆) lattices, and the transformation of MoO₂ to the stoichiometric MoO₃ phase at $T = 600^\circ\text{C}$. Theoretically, the weight gain for the conversion of MoO₂ to MoO₃ was approximately 12.5%. From the TG analysis, it was observed that the weight of the sample increased by ≈10.4% from room temperature to 600°C in the air. Thus, the calculated value for conversion of MoO₂ and

the suboxides (i.e., Mo_4O_{11} , Mo_8O_{23} and Mo_9O_{26}) to the stoichiometric MoO_3 is close to the theoretical value. It is worth noting that the color of MoO_2 was black before the TG measurements and converted to the color yellow after the TG runaway to 600 °C. In addition, this TG of MOV confirmed that there was no carbon coating around their particles. This was because there was no weight loss above 500 °C related to the emission of CO_2 as a result of the reaction between oxygen in the air and carbon, if present. However, some mass loss might occur, which was masked by oxygen gain during the oxidation process.

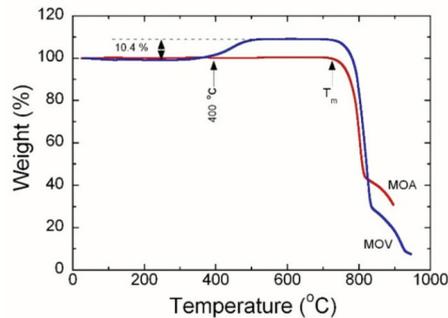


Figure 3. Thermogravimetry (TG) curves of the MOA and MOV samples recorded at a heating rate of 10 °C min^{-1} . MOA displays the typical behavior of the stoichiometric MoO_3 orthorhombic phase, while MOV shows the oxidation of the suboxide at 400 °C and the conversion to MoO_3 at 600 °C.

The SEM images (a–c) and TEM image (d) of the MOA and MOV samples depicted in Figure 4 illustrate the influence of the synthesis conditions on the particle size and morphology. There is a significant difference between the morphology of molybdenum oxide prepared in air and that prepared in vacuum from the same ammonium molybdate tetrahydrate precursor. Air calcination gives heterogeneous MOA particles with well-crystallized crystals a platelet-like shape (Figure 4a,c). The sizes of the MOA particles were in a wide range from the sub-micrometer to $\sim 10\text{ }\mu\text{m}$ [71]. On the contrary, calcination in vacuum provided homogeneous MOV powders with an ash-like morphology at the nanometer size (Figure 4b). SEM (Figure 4c) and TEM images (Figure 4d) show that the MOA platelets had sizes larger than $1\text{ }\mu\text{m}$, while the MOV powders had smaller sizes, in the 40–100 nm range. The size and morphology differences of the MOA and MOV particles were mainly due to the heat treatment conditions.

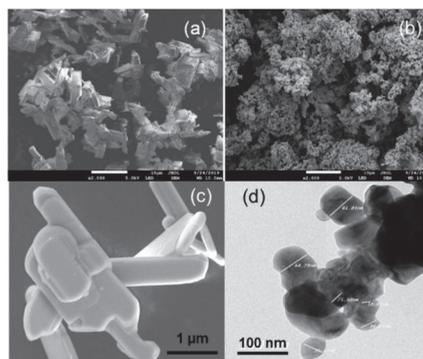


Figure 4. (a,b) SEM images of the MOA and MOV samples synthesized using a sol-gel method assisted by a biological chelator (scale bar of $10\text{ }\mu\text{m}$). (c) Magnified SEM image of the MOA (scale bar of $1\text{ }\mu\text{m}$) and a (d) TEM image of the MOV sample (scale bar of 100 nm).

Raman spectroscopy is a sensitive tool for investigating the coordination, structure, lattice vibrations, and symmetry of molybdenum and oxygen atoms in the presence of different phases. Further structural analyses of as-prepared molybdenum oxides were carried out by Raman scattering spectroscopy using the excitation line at $\lambda_{\text{exc}} = 532 \text{ nm}$ (Figure 5a–d). The Raman spectrum of the MOA sample (Figure 5a) displays the typical vibrational features of the orthorhombic $\alpha\text{-MoO}_3$ phase. Twelve vibrational modes were evidenced by the peaks located at 197, 216, 245, 283, 290, 336, 364, 378, 471, 665, 818, and 995 cm^{-1} . The wavenumbers and relative intensities matched closely with the single crystal Raman spectrum given in the literature [72–76]. Most of the Raman active modes were dominated by either interlayer or intralayer contributions. More specifically, the peak at 665 cm^{-1} was related to the $\nu(\text{O-Mo}_3)$ stretching mode of the triply-coordinated oxygen atoms, which are shared by three MoO_6 octahedra. The intense peak at 818 cm^{-1} was linked to the doubly-coordinated oxygen $\nu(\text{O-Mo}_2)$ stretching mode. The high-wavenumber peak at 995 cm^{-1} was associated with the $\nu(\text{Mo}^{6+}=\text{O})$ asymmetric stretching mode of terminal singly-coordinated (unshared) oxygen atoms, which had bonds that were responsible for the layered structure of the $\alpha\text{-MoO}_3$ orthorhombic phase [75]. Figure 5b–d presents the micro-Raman spectra of the MOV sample recorded on different areas of the sample using 1% laser power (0.5 mW) at a 532 nm laser-line excitation. The micro-Raman results were in good agreement with the XRD findings. The mixture of vibrational features of the MoO_2 and $\text{Mo}_n\text{O}_{3n-1}$ suboxide phases (i.e., $o\text{-Mo}_4\text{O}_{11}$, $m\text{-Mo}_8\text{O}_{23}$, $o\text{-Mo}_9\text{O}_{26}$ Magnéli) can be identified [77–83]. The Raman bands of the MOV sample located at 126, 203, 228, 346, 362, 458, 470, 495, 570, 585, and 741 cm^{-1} (Figure 5b) correspond to a rutile-type (monoclinic) structure and agreed well with the vibrational features of the $m\text{-MoO}_2$ reported in the literature [77–80]. Two weaker peaks, located at 425 and 820 cm^{-1} , were attributed to the orthorhombic $o\text{-Mo}_4\text{O}_{11}$ suboxide [81,83].

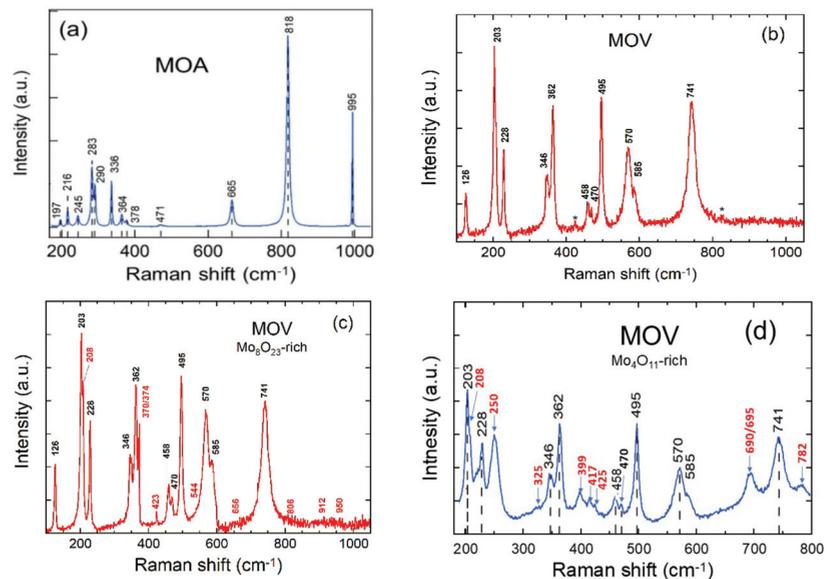


Figure 5. Raman spectra of the (a) MOA powders, (b) MOV (MoO_2 -rich sample where the stars correspond to Raman peaks of suboxides), (c) MOV with $m\text{-Mo}_8\text{O}_{23}$ -rich particles, and (d) MOV with $o\text{-Mo}_4\text{O}_{11}$ -rich particles. Spectra were recorded at a spectral resolution of 1 cm^{-1} .

Vibrational analysis of the MoO_2 spectrum reveals that the bands in the 500–800 and $200\text{--}400 \text{ cm}^{-1}$ regions were due to Mo–O stretching and bending modes, respectively. The low-frequency region ($<200 \text{ cm}^{-1}$) corresponded to the lattice modes. The Raman spectra

of suboxide-rich areas are displayed in Figure 5c,d for the MOV with m-Mo₈O₂₃-rich and o-Mo₄O₁₁-rich particles, respectively (Raman peaks of suboxides are marked in red). The monoclinic m-Mo₈O₂₃ phase is identified through the Raman peaks at 208, 370/374, 656, 912, and 950 cm⁻¹, whereas peaks located at 208, 250, 325, 399, 417, 425, 695, 782, 806, and 912 cm⁻¹ are assigned to the o-Mo₄O₁₁ phase. Moreover, the MOV sample contained a small amount of the o-Mo₉O₂₆ suboxide identified by the peaks at 208, 544, 782, 912, and 950 cm⁻¹. The spectroscopic results are listed in Table 2 and compared with the literature data [81,82].

Table 2. Reported Raman peak frequencies (cm⁻¹) of M–O oxides.

α-MoO ₃		m-MoO ₂		o-Mo ₄ O ₁₁		m-Mo ₈ O ₂₃		o-Mo ₉ O ₂₆	
Exp.	[81]	Exp.	[82]	Exp.	[82]	Exp.	[82]	Exp.	[82]
197	-	126	-	208	208			208	208
216	217	203	208	250	253	208	208	-	465
245	245	228	232	-	281	-	222	544	575
283	284	346	353	325	339	374	373	-	622
290	291	362	370	399	380	-	384	-	637
336	338	458	448	417	413	-	592	-	679
364	365	470	473	425	435	656	654	782	761
378	379	495	501	695	714	-	875	912	906
471	472	570	572	782	787	912	918	-	931
665	666	585	590	806	837	950	951	950	951
818	820	741	748	912	916			-	989
995	996			-	963				

XPS measurements were carried out to evaluate the chemical composition and investigate the surface valance states of Mo in MOA and MOV samples. The results are shown in Figure 6. The survey spectra (Figure 6a) display the fingerprints of the Mo 3d, Mo3p_{3/2}, Mo3p_{1/2}, and O1s core levels (their binding energies are listed in Table 3). The Mo 3d and O1s peaks were analyzed by evaluating the peak area of elements using Gaussian profiles after removing the secondary electron background. All XPS spectra can be deconvoluted using two Mo 3d doublets with 3d_{5/2} and 3d_{3/2} species. For the MOA sample (Figure 6b), the Mo 3d_{5/2} and Mo3d_{3/2} characteristic peaks were located at 232.6 and 235.7 eV, respectively (with a spin–orbit separation of ~3.1 eV), suggesting the sole existence of Mo⁶⁺ species on the MOA surface [23,84,85]. The binding energy of the Mo 3d_{5/2} line for polycrystalline MoO₃ has been reported to be 231.6–232.7 eV [86–88]. For the MOV sample, the deconvoluted peaks in Figure 6c unambiguously reveal the co-existence of mixed Mo valence states (Table 3).

Table 3. XPS analysis of the MOA and MOV samples.

Sample	Binding Energy (eV)									Average Mo Valence State
	Mo3p _{3/2}	Mo3p _{1/2}	O1s	Mo3d _{5/2}			Mo3d _{3/2}			
				Mo ⁴⁺	Mo ⁵⁺	Mo ⁶⁺	Mo ⁴⁺	Mo ⁵⁺	Mo ⁶⁺	
MOA	398.9	415.5	530.5	-	-	232.6	-	-	235.7	6.00
MOV	398.9	415.5	530.6	233.1	230.0	231.6	236.3	233.3	234.7	4.39

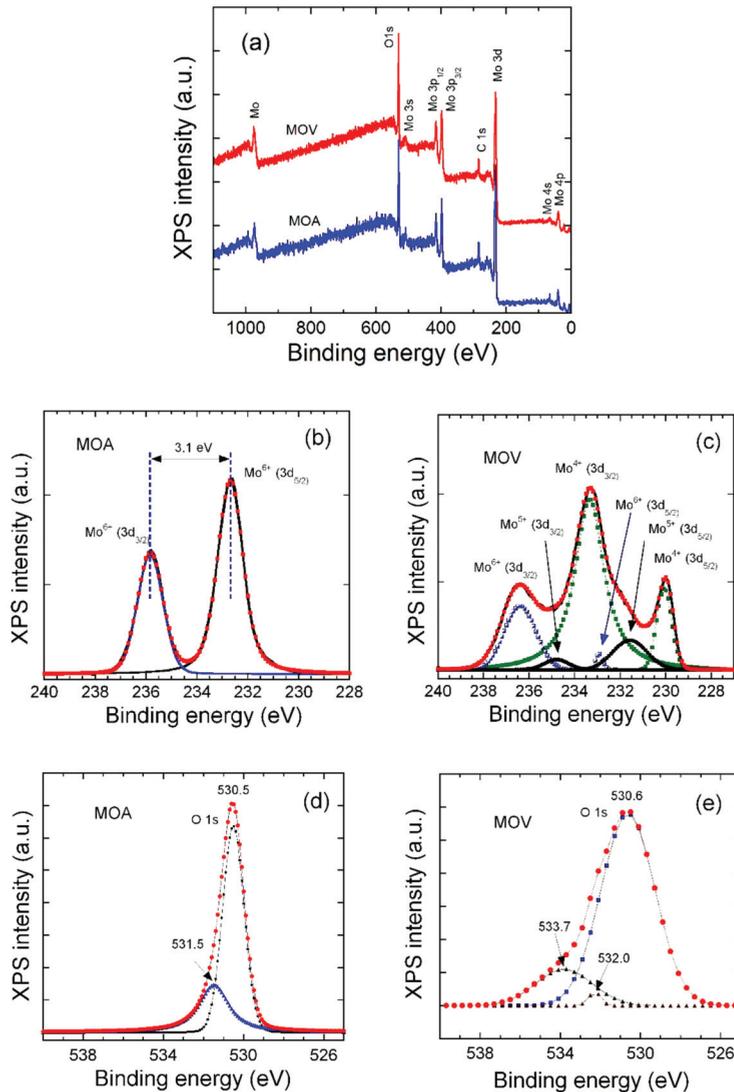


Figure 6. (a) XPS survey spectra of the MOA and MOV samples. High-resolution XPS spectra of (b) Mo 3d in MOA, (c) Mo 3d in MOV, (d) O1s in MOA, (e) O1s in MOV.

The first doublet centered at 230 and 233.3 eV was typically the Mo 3d_{5/2} and Mo 3d_{3/2} of Mo⁴⁺, respectively, whereas the second one located at 231.6 and 234.7 eV was due to the Mo⁵⁺, and, finally, the last one located at 233.1 and 236.3 eV was due to the Mo⁶⁺ [88,89]. The XPS spectra of O1s are presented in Figure 6d,e for the MOA and MOV samples, respectively. The intense peak located at $\sim 530.5 \pm 0.1$ eV was attributed to the binding energy of Mo–O bonds, whereas the peak at a higher binding energy was assigned to surface states. Therefore, the surface states of the MOV observed in the XPS patterns ascribed the presence of MoO₂, Mo₄O₁₁, Mo₈O₂₃, and Mo₉O₂₆ (Figure 6c). From XPS peak deconvolution, the average Mo valence state of the MOA and MOV sample was determined to be 6.00 and 4.39, respectively.

The porous texture of the MOA and MOV samples was investigated by the N₂ adsorption–desorption isotherm measurement. The isotherm profiles of samples can be categorized as a type IV curve with a H3 hysteresis loop at the relative pressure of 0.8–1.0, thus implying the existence of a large number of mesopores. The average pore size was below 2 nm in the MOV material, while the MOA sample exhibits an average pore size of 10 nm. Moreover, the Brunauer–Emmett–Teller (BET) specific surface area of the MOV was 4.0 m² g^{−1}, which was higher than that of the MOA (0.23 m² g^{−1}). The mesoporous structure of the Mo–O samples may be beneficial for the electrolyte to penetrate completely into the pores and diffuse efficiently to active sites with less resistance, and can also buffer large volume change during the Li⁺-ion insertion/extraction processes. The equivalent particle size of the MOA and MOV samples can be calculated from the BET data and compared using SEM images. The average particle size (nm) is expressed by Equation (6) below [90]:

$$L_{\text{BET}} = \frac{6000}{S_{\text{BET}}d'} \quad (6)$$

where S_{BET} is the specific surface area (in m² g^{−1}) measured by BET experiments, and d' is the gravimetric density (4.70 and 6.47 g cm^{−3} for MoO₃ and MoO₂, respectively). Results of the sample texture are summarized in Table 4. Note that the L_{BET} values corresponded to the average size of the secondary particles (agglomerates observed in SEM images).

Table 4. BET specific surface area (S_{BET}) and average pore size and pore volume of the MOA and MOV samples.

Sample	S_{BET} (m ² g ^{−1})	Pore Size (nm)	Pore Volume (cm ³ g ^{−1})	L_{BET} (nm)
MOA	0.23	10	0.0012	3500
MOV	4.00	~2	0.0002	231

3.2. Electrochemical Properties

The electrochemical properties of as-prepared MOA and MOV as anode materials of LIBs were investigated in a potential range of 0.01–3.0 V vs. Li⁺/Li. Figure 7a shows the cyclic voltammetry (CV) curves of MoO₃ performed at a scanning rate of 0.01 mV s^{−1}. MoO₃ demonstrates four prominent peaks in the first discharge process located at 2.7, 2.28, 0.7, and 0.3 V. The peaks at 2.7, 2.28, and 0.7 V appear only in the first discharge cycle and disappear in the subsequent cycles. This feature has been attributed to the intercalation of Li ions into the interlayer space between MoO₆ slabs, which occurs as the Li_xMoO₃ phase (see Equation (1)) and causes irreversible structural change to MoO₃ in a lithiated amorphous phase [91]. The peak at 0.3 V originates from a conversion reaction (see Equation (2)) of Li_xMoO₃ to Mo⁰ and Li₂O [92]. The shift to a rather low voltage for the peak at 0.3 V with subsequent cycles may be attributed to a structure evolution. Two broad anodic peaks observed at approximately 1.18 and 1.73 V correspond to the de-lithiation process and are maintained in the forthcoming cycles. Note that the strong cathodic peak slightly shifts by 0.25 V after the first cycle. Figure 7b displays the galvanostatic charge–discharge profiles of the MOA sample. The upper voltage discharge plateau, observed in the first discharge, disappear in the subsequent cycles and the plateau at approximately 0.3 V shifts to lower voltage as noticed in CV results. These electrochemical features are those of the MoO₃ phase reported so far [93]. At 1C-rate (current density of ~1.1 A g^{−1}), the discharge capacity of the MoO₃ electrode decreased abruptly from the initial value of 1613 to 330 mAh g^{−1} over the first 50 cycles and then slightly increased in subsequent discharge–charge cycles at a rate of 0.35 mAh g^{−1} per cycle, reaching the specific capacity of 435 mAh g^{−1} after 725 cycles (Figure 7c). The Coulombic efficiency remained almost at 100% during long-term cycling. The initial large capacity decay revealed the poor electrochemical stability of MoO₃ electrode, which was due to the huge volume expansion and/or the structural change during the conversion reaction [91]. The rate capability displayed in Figure 7d for MOA

showed significant capacity fading upon increasing the loading current. Moreover, after returning to the initial low C-rate (0.1C), the capacity did not return to its initial value and lost more than half of its value.

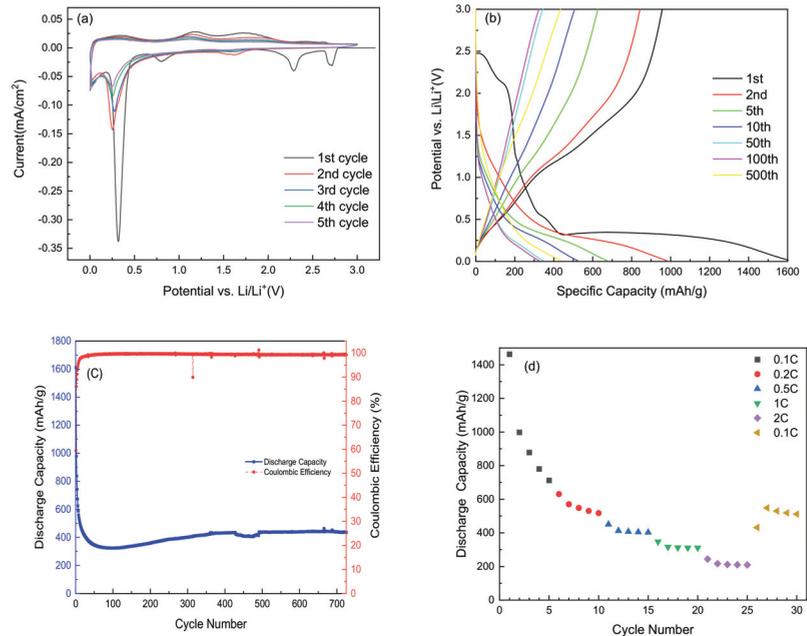


Figure 7. Electrochemical performance of MOA as anode material: (a) five first cyclic voltammograms recorded at 0.01 mV s^{-1} scanning rate, (b) galvanostatic charge/discharge curves carried out at 1C-rate ($\sim 1.1 \text{ A g}^{-1}$) in the potential window 0.01–3.0 V vs. Li^+/Li , (c) specific discharge capacity and Coulombic efficiency as a function of cycle numbers performed at a 1C-rate, and (d) rate capability.

Figure 8a shows the first five cyclic voltammograms of the MOV electrode material, which exhibited five cathodic peaks located at 2.03, 1.53, 1.25, 0.78, and 0.42 V vs. Li^+/Li . Note that the cathodic peaks located at 2.03 and 0.78 V disappeared starting from the 2nd cycle, and it may be related to the reduction in solution species and formation of a solid electrolyte interphase (SEI) on the anode surface, while the one at 0.42 V shifted to lower potential. The two strong cathodic peaks at 1.25 and 1.53 V were maintained in the subsequent cycles with a slight shift toward higher potentials (1.27 and 1.56 V, respectively). This high potential shift makes them close to the two strong anodic peaks at 1.43 and 1.7 V. A decrease in the potential difference ΔE between the redox peaks started from the 2nd cycle to 0.16 and 0.14 V instead of 0.18 and 0.17 observed in the 1st cycle. In the subsequent cycles, these voltage sets 1.27/1.43 and 1.56/1.7 V were assigned to the reversible phase transitions (monoclinic–orthorhombic–monoclinic) of partially lithiated Li_xMoO_2 during Li intercalation (discharge) and de-intercalation (charge) processes, which are in a good agreement with previous reports [92–95].

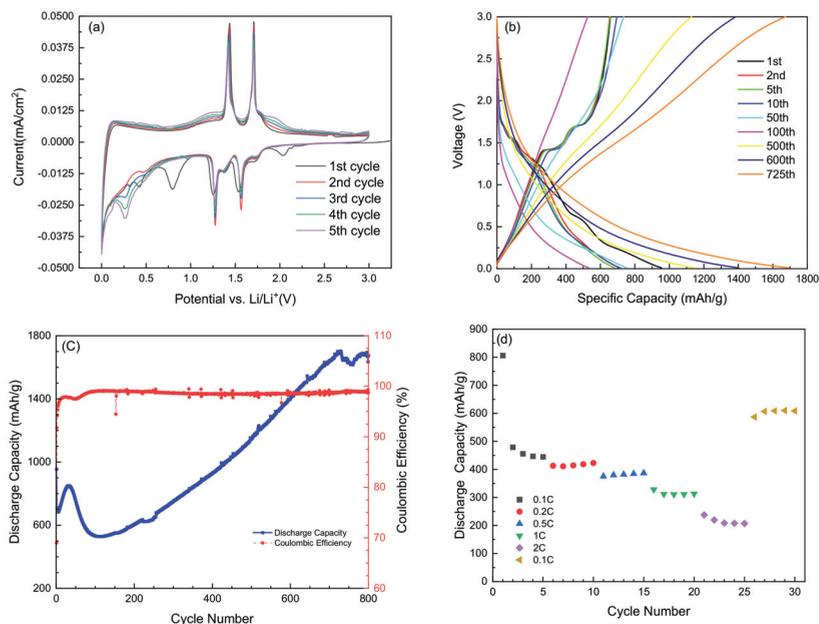


Figure 8. Electrochemical performance of MOV as anode material. (a) First five cyclic voltammograms recorded at scanning rate of 0.01 mV s^{-1} . (b) Galvanostatic charge/discharge curves of MoO_2 performed at 1C-rate ($\sim 0.86 \text{ A g}^{-1}$). (c) Specific discharge capacity and Coulombic efficiency as a function of cycle number performed at 1C-rate. (d) Rate capability.

It is worth noting also that the CV curves starting from the 2nd cycle to the 5th cycle almost overlapped. This demonstrates that the as-prepared material (i.e., the mixture of MoO_2 and $\text{Mo}_n\text{O}_{3n-1}$ suboxides) had good stability and reversibility for lithium-ion insertion and extraction during the first several cycles. Figure 8b illustrates the galvanostatic discharge–charge profiles of the MOV anode material tested at 1C-rate ($\sim 0.86 \text{ A g}^{-1}$) in a potential window 0.01–3.0 V vs. Li^+/Li . Two prominent plateaus at 1.25 and 1.53 V were observed during discharge process besides other small plateaus. The first lithiation mechanism was an insertion-type reaction that took place in the bulk and amorphous MoO_2 electrodes with only one-electron reduction as described (see Equation (3)) [46]. The second step was a conversion reaction that gradually resolved Li_xMoO_2 as described by Equation (4) [47], showing the formation of metallic Mo and Li_2O . In the charge curve, two plateaus were evidenced at 1.43 and 1.70 V and assigned to the deintercalation of Li^+ from Li_xMoO_2 framework. The disappearance of small plateaus starting from the 2nd cycle is related to an irreversible structural change suggesting that part of Li^+ cannot be extracted during the charge process [69]. Starting from the 2nd cycle, discharge and charge redox plateaus were clearly observed as noticed in the cyclic voltammograms. A voltage upgrading was detected upon cycling the MoO_2 phase, which did not exist for MoO_3 . Figure 8c exhibits the electrochemical performance of the MOV anode material cycled at 1C-rate. An initial discharge capacity around 900 mAh g^{-1} was delivered in the 1st cycle, which decreased to $\sim 500 \text{ mAh g}^{-1}$ after 100 cycles and then increased on subsequent cycles reaching a value of 1625 mAh g^{-1} after 700 cycles. The Coulombic efficiency increased also from 93% to almost 99.4% after 100 cycles. This better electrochemical behavior of the MOV electrode in comparison with that of MOA is attributed to several factors: (i) the smaller size of the nanoparticles, (ii) the presence of highly conductive suboxide phases, (iii) the higher BET specific surface area, (iv) the high intrinsic electrical conductivity of the MoO_2 phase, and (v) the meso-porosity. The importance of cycling at a high C-rate

was also evidenced in Figure 8d, showing the rate capability of the MOV electrode. The rate capability of the MOV electrode is shown in Figure 8d. When the C-rate increased from 0.1C to 2C, the discharge capacity decreased from approximately 450 mAh g⁻¹ to approximately 200 mAh g⁻¹. However, when the rate returned back to 0.1C after 2C testing, the capacity also returned back to approximately 600 mAh g⁻¹, which is slightly higher than the capacity during the initial 0.1C test. This slight increase was consistent with the capacity change pattern shown in Figure 8c. The capacity slightly increased from the 5th cycle to about the 50th cycle.

The gradual increase in the discharge capacity and additional capacities beyond the correlating theoretical value upon long-term cycling is worthy to be discussed. This characteristic is common in a large number of conversion reaction metal-oxide anode materials [96–106]. Keppeler and Srinivasan stated that the mechanism leading an experimental capacity larger than the theoretical value remains speculative [98]. The literature reveals a lithium storage capacity higher by 10–100% at high current densities of 30–2000 mA g⁻¹ after being tested beyond 50 cycles [96,97]. Different capacity shapes have been reported that exhibit additional capacity occurrences. Cobalt oxides frequently show a type I (mount-shape) capacity profile [99], type II (upward-shape) is observed for additional capacity occurrence for Fe- or Mn-oxide-based electrodes [100], type III (U-shape) is a typical capacity profile found for several cases when the anode material contains Mn or Fe [101], and iron-oxide-based electrodes tend to form a type IV (horizontal-shape) capacity profile [96]. Here, the MOV negative electrode material exhibited a capacity profile type III with a pronounced U-shape. The specific discharge capacity was almost twice the theoretical value after 800 cycles monitored at a high 1C-rate with a Coulombic efficiency, which remained constant at 99.4%. This is in contrast with the type IV profile reported by Shi et al. [102] for the mesoporous MoO₂ electrode synthesized at 500 °C via a nanocasting strategy. However, the self-assembled porous MoO₂/graphene microspheres, fabricated by Palanisamy et al. [103], exhibited a weak U-profile when cycled at a low current rate (C/10). A different capacity profile (upward-shape) was reported by Tang et al. [104] for an MoO₂-graphene nanocomposite electrode cycled at 100 mA g⁻¹. Thus, not only the morphology plays an important role in the excess capacity but also the operating mode is modifying the electrochemical performance upon long-term cycling of nanostructured oxides.

After the 100th test, the MOV anode displayed a gradual increase in specific capacity during cycling (Figure 8c). This anomalous behavior can be attributed to: (i) the activation of the porous structure with nano-cavities; the presence of numerous mesopores might be beneficial for the gradual access of the electrolytes in the porous structure of the electrode, and (ii) an additional Li-ion accommodation through reactions with the grain boundary phase in nanostructures; other scenarios associated with additional capacities, such as electrode/electrolyte interphases and electrocatalytic effect of metallic particles, have been identified [98]. The existence of numerous mesopores might be beneficial for more electrolytes accessing in the porous framework of the electrode, which favors the Li⁺ insertion/extraction process. Such a characteristic was evidenced in cobalt-based anodes [105], MnO/graphene composite [100], and graphene-wrapped Fe₃O₄ [106]. In MnO_x anodes, it might be based on mixed effects such as transition-metal cluster aggregation and formation of defects and deformation [101].

Table 5 summarizes the electrochemical performance of various MoO₂ anode materials prepared by various synthetic processes [107–125]. The different strategies demonstrate the ability to mitigate the particle pulverization as a consequence of Li insertion/extraction and improve the MoO₂ electrochemical performance via the fabrication of nanocomposites including carbonaceous materials. The particle size reduction results in the transport path shortening for both ions and electrons, while the carbonaceous matrix maintains high conductivity, large surface area, and chemical stability. The MoO₂-based composites studied as lithium battery anodes involve various forms including mesoporous and monolith MoO₂; nanostructured powders such as nanowires (NWs), nanospheres (NSs), hollow spheres (HSs), and nanobelts (NBs); MoO₂/carbon materials; various binary composites. Thermo-

electrochemical activation of MoO₂ is also an attractive synthetic approach. A comparison of the electrochemical properties of these anode materials shows that the MoO₂/Mo_nO_{3n-1} composite prepared by a simple sol-gel technique assisted by a green chelator exhibits the best performance.

Table 5. Electrochemical performance of various MoO₂ composites as anode materials for LIBs. The cycle number at which the specific capacity is reported is given in parenthesis.

Material	Synthesis	Reversible Capacity (mAh g ⁻¹)	Current Rate (mA g ⁻¹)	Reference
Nano MoO ₂	rheology	402	100 (40)	[118]
MoO ₂ /Mo ₂ N	reduction of MoO ₃	815	100 (150)	[119]
MoO ₂ /graphene	chemical vapor deposition	986	50 (150)	[120]
MoO ₂ /C	ion exchange	574	100 (100)	[121]
MoO ₂ /C	carbothermal reduction	500	100 (50)	[108]
MoO ₂ /C hollow spheres	solvothermal	580	200 (200)	[122]
Mesoporous MoO ₂	template casting	750	42 (30)	[103]
Activated MoO ₂	thermoelectrochemical activation	850	100 (30)	[123]
MoO ₂ HCSMSs	hydrolysis	420	50 (30)	[124]
W-doped MoO ₂	nanocasting	670	75 (20)	[111]
C/WO _x /MoO ₂	hydrothermal	670	90 (50)	[125]
MoO ₂ /C NWs	solvothermal	500	200 (20)	[109]
C/MoO ₂ NSs	hydrothermal+annealing	675	838 (30)	[113]
MoS ₂ /MoO ₂	sulfur assisted	654	500 (80)	[115]
C/MoO ₂ NBs	hydrothermal+annealing	617	100 (30)	[110]
MoO ₂ monolith	morphosynthesis	719	200 (20)	[112]
α-MoO ₃ @β-MnO ₂	two-step hydrothermal	286	6C (50)	[107]
MoO ₂ /N-doped C NWs	calcination	700	2000 (400)	[114]
C-coated MoO ₂	hydrothermal	312	10000 (268)	[116]
MoO ₂ /flexible C	electrospinning	451	2000 (500)	[117]
MoO ₂ /Mo _n O _{3n-1}	sol-gel with green chelator	1600	800 (800)	this work

To further investigate the electrochemical kinetics as well as characterize the improved electrochemical properties of MOA and MOV negative electrode materials, EIS measurements were carried out using a fresh cell. Figure 9a shows the Nyquist plots for the MOA and MOV electrodes. The equivalent circuit model (Figure 9b) used to analyze the EIS results is composed of a series of four elements: the cell resistance R_s , a resistance in parallel with a constant phase element corresponding to the solid electrolyte interphase (SEI) layer, a second R - CPE parallel component, which figures out the charge transfer process, and finally the diffusion Warburg component (Z_W). All Nyquist plots can be decomposed as follows: (i) the intercept at high frequency with the Z' -axis is related to the uncompensated ohmic resistance of the cell (R_s); (ii) in the high-frequency region, the first depressed semicircle is associated with the SEI (R_{SEI} , CPE_{SEI}); (iii) a second depressed semicircle in the medium-frequency region is ascribed to the charge transfer impedance and the interfacial capacitance at the electrode/electrolyte interface (R_{ct} , CPE_{dl}); finally, (iv) in the low-frequency range, the inclined line is ascribed to the Li⁺-ion diffusion-controlled process characterized by the Warburg impedance. The values of R_s for the two samples are quite small ($\sim 7 \Omega$) implying a negligible ohmic polarization of the MOA and MOV electrodes. The R_{ct} value is lower in the MOV material (211 Ω) compared to the MOA (272 Ω) electrode. This matches well with the electrochemical performance of MOV mentioned above. This is attributed to the presence of Mo suboxides in MOV electrode (mixture of MoO₂, o-Mo₄O₁₁, m-Mo₈O₂₃, and o-Mo₉O₂₆), which leads to a significant increase in the electronic conductivity as compared to MOA.

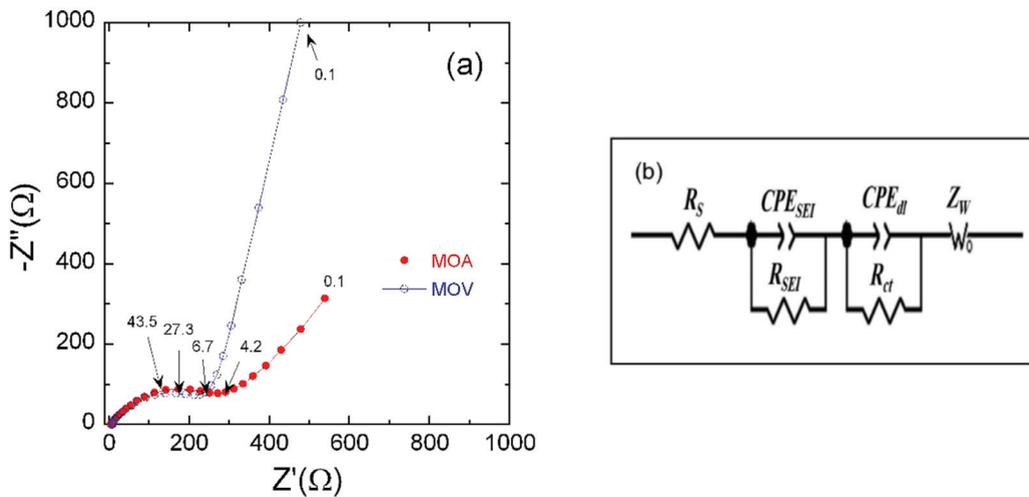


Figure 9. (a) Nyquist plots of fresh cells including the MOA and MOV electrodes. (b) The equivalent circuit model used for EIS data fitting.

More information on the change in the overall cell potential as a function of the depth-of-charge (DOD) can be obtained by evaluating the area-specific impedance (ASI expressed in $\Omega \text{ cm}^2$) given by the relation [126,127]:

$$ASI = A \frac{OCV - V_{cell}}{I}, \tag{7}$$

where A is the cross-sectional area of the electrode, $\Delta V = OCV - V_{cell}$ is the potential change during current interruption for 60 s at each DOD step, and I is the current passing throughout the cell. ASI is affected also by ohmic drop, Li-ion diffusion through the electrolyte and solid-state diffusion within the electrode. This is like EIS measurements without the need to reach the equilibrium. Moreover, ASI could be more representative than data from EIS in terms of evaluation of the total cell resistance. However, ASI results confirmed the features observed by EIS. Figure 10a displays the variation of ASI for the MOA and MOV electrodes for the 1st discharge at 1C-rate. ASI values at 90% DOD are 22 and 16 $\Omega \text{ cm}^2$ for the MOA and MOV samples, respectively. The curves in Figure 10a indicate that, during battery discharging, the charge–transfer resistance is dependent on DOD. To further verify the effect of ASI on the electrochemical properties of MOA and MOV electrodes, ASI was calculated at various discharge cycles at 20% and 90% DOD as shown in Figure 10b. These results show that there were two different behaviors represented by an increase in the ASI values during the first five cycles, followed by a continuous decrease until the 725th cycle. The degree of decay in ASI values was much larger for MOV than for MOA at 20% DOD. By going to a deep discharge of 90% DOD, the situation looks rather different. ASI values increased after the 1st cycle then almost stabilizes until the 725th cycle for the MOA electrode. On the contrary, MOV showed smaller ASI values than MOA with a continuous reduction upon cycling upon shallow discharge (20% DOD). These results show that the lower ASI value was obtained for the MOV sample, and it is beneficial for the long-life cycling behavior.

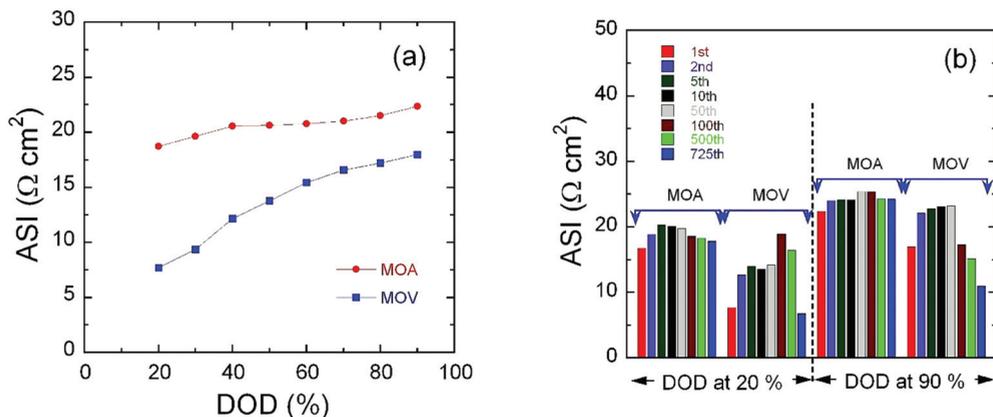


Figure 10. Area specific impedance (ASI) of the MOA and MOV as a function of depth of discharge (DOD) for the 1st discharge (a) and as a function of cycling for the MOA and MOV electrodes at 20% and 90% DOD (b).

4. Conclusions

This research article sheds light on the promising design strategies of molybdenum oxides for high kinetic energy storage. The green and facile preparation of nanosized molybdenum oxides (i.e., MoO_3 and MoO_2) by thermal decomposition of ammonium molybdate tetra hydrate (i.e., $(\text{NH}_4)_6\text{Mo}_7\text{O}_{24}\cdot 4\text{H}_2\text{O}$) in air and in an inert atmosphere, respectively, has been demonstrated. The efficiency of the synthetic method is attributed to the use of orange peel extract as a chelator. The as-prepared MOA and MOV materials have the structure of MoO_3 and $\text{MoO}_2+\text{Mo}_n\text{O}_{3n-1}$ suboxides as estimated from XRD, XPS, and Raman spectroscopy. Thermal analysis emphasized the thermal stable phase of MoO_3 up to approximately 800°C and the presence of oxygen vacancies in the MOV sample. BET measurements show the mesoporous texture of molybdenum oxides; MOA had a lower specific surface area than MOV due to the easy crystal growth in the MoO_3 phase. Electrochemical characterizations showed the outstanding properties in terms of capacity upgrading upon cycling for the MOV negative electrode material, which shows a pronounced U-shape capacity profile when cycled 800 times at 1C-rate. Finally, EIS and ASI experiments confirmed the superiority of the MOV (mixture of MoO_2 , Mo_4O_{11} , Mo_8O_{23} , and Mo_9O_{26} phases) over the MOA (stoichiometric MoO_3 insulator) sample as an anode material for Li-ion batteries.

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